

1 Introduction

The design and development of flying platforms is not a new concept, it has been an ongoing task by the United States military since 1964 [1]. Billions of dollars have been spent researching and developing uninhabited (or unmanned) aerial vehicles (UAVs) for a variety of different purposes.

In the military field, UAVs could be considered as a cost-effective alternative for important missions such as gathering electro-optical information, delivering munitions, deceiving and jamming radars, and as targets for missile tests [2]. Civil applications of UAVs are providing topographical data for geographical researches, agricultural spraying, meteorological measurements at high altitude, pollution studies, traffic reports and a large range of other applications [3].

Many of the applications above use or obtain information. There are currently two ways in which UAVs can relay information. The first is by the use of wireless communications such as satellite communication, this method is currently being utilised by UAVs such as the RQ-3A DarkStar Tier III Minus [4] and Predator [5]. The second is by information storage to a hard drive of some description which can then be read upon return of the UAV. This is currently being used by the Australian military to track "rebels" and "gangs of thugs" on the Solomon Islands, it is used as it is more secure than sending transmissions that may be intercepted [1].

UAVs are more preferable to manned aircraft as a result of the reduced expenses and a lesser restriction of flight destinations. For example, fuel costs are generally lower, there are no pilot costs, and they are able to enter toxic environments with no major cause for concern. For these reasons and many others the UAV market is expected to grow by a compound annual growth rate of 12.2% and have an annual revenue of \$6.78 billion by the year 2008 [6]. Therefore the importance and relevance to real world applications can be seen and forms good reason to undertake this project. Further information on UAVs is discussed in Section 2.2.

This project is a continuation of the work that has been undertaken by students at the University of Exeter since 2001. Its final goal is to design and develop an autonomous unmanned aerial vehicle (AUAV). The work set was based on the suggestions formulated by the 2003 group. Its aims were to adapt the current design to enable an on board power supply, use an IC engine, and increase the reliability of the control system.

This report covers the management of the project, aspects of propulsion, and then concentrates on control sensor manipulation.

2 Background Research

The concept of an autonomous flying platform is not new, however it is a difficult concept to grasp when approaching the field of avionics for the first time. Therefore before work was set on project objectives, background research was necessary to give an indication of what aspect will be involved in the design and development of flying platforms. Thus the project reports of the previous years were analysed and an internet search on current UAVs were performed.

2.1 Flying Platform Definition

The definition of a flying platform as stated by [7] reads “a device that can take off vertically, can hover, and has a gross weight of less than 1000 lbs”. The definition of autonomous is “Able to act independently. In the case of Swift, this means that the spacecraft can reprogram itself without ground controllers feeding it commands” [8]. This implies that there must be an incorporation of a propulsion and control system which must work in unison to achieve the overall objective of stable flight. The next section will discuss current UAVs their purpose and other important factors.

2.2 Unmanned Aerial Vehicles (UAVs) to Date

UAVs can be either autonomous or semi-autonomous i.e. controlled remotely. The area that this project is concerned with is autonomous, although some semi-autonomous UAVs can provide the necessary scope to enable a better understanding of certain operations.

2.2.1 RQ-2 Global Hawk

The "R" is the Department of Defence designation for reconnaissance; "Q" means unmanned aircraft system. The current range is RQ-1 to RQ-7. Each Global Hawk costs \$15 million to manufacture. This UAV is over 40 feet long, and thus requires a very large run-way for take-offs and landings. Controlled by a human operator, not an on-board computer, the Global Hawk can stay in the air for as long as 40 hours. In that time, and without stopping once to re-fuel, it can travel 3,000 miles to its target, focus upon an area of up to 3,000 square miles, from as high up as 65,000 feet. This area can be analysed by the use of electro-optical, infra-red and Synthetic Aperture Radar (SAR) cameras to take pictures of the ground. This information can then be used via wireless technology or satellites to transmit those pictures in "real time"; and then return back to its base station. The Global Hawk was first used by the Department of Defence to help NATO bombers spot potential targets in the 1998 war over Kosovo [1]. A picture of the Global Hawk can be seen in Figure 2.2.1.1.



Figure 2.2.1.1. Global Hawk [1]

2.2.2 General Atomics' RQ-1 Predator

The Predator as shown in Figure 2.2.2.1 is quite similar to the Global Hawk, it also requires a human operator and a long run-way for take-offs and landings. But at \$4.5 million each, the 27-foot-long Predator is cheaper and smaller [5]. As a result, it is worth the risk of being sighted and shot-down which explains why the Predator is normally flown at relatively low altitudes of 25,000 feet and below. Predators were first deployed for reconnaissance and surveillance operations ("RQ-1") by the US military during the 1995 civil war in Bosnia. Since then Predators have been used more extensively, for instance the USA's assault on Afghanistan in October 2001 [9]. Although they were not used in the March 2003 assault on Iraq as 12% of them crashed in 2001 as a result of bad weather and technical problems [9].



Figure 2.2.2.1. Predator [5]

2.2.3 Sikorsky's Cypher

The Cypher as shown in Figure 2.2.3.1 can be relatively small with some versions only being 8 feet tall, 3 feet wide, and a weight of 30 pounds, which allow it to enter buildings as well as hover above or land on top of them [9]. The uniqueness of the Cypher isn't simply a matter of its small size and manoeuvrability. Unlike the Global Hawk and the Predator, the Cypher is a fully automated uninhabited spy plane, it simply needs to know where to go to find its targets. Once given this information, the Cypher can launch itself vertically, like a helicopter and can use the military's network of Global Positioning Satellites (GPS) to find out where its launch has placed it. It uses a variety of on-board cameras to see where it needs to go, and purposely built internal computer programs to inform it that it has reached its destination, what to do, and when to return to the base station [10].



Figure 2.2.3.1. Cypher [1]

2.2.4 RQ-3 Darkstar

The DarkStar as shown in Figure 2.2.4.1 was a low observable tactical reconnaissance UAV designed by The Lockheed Martin Skunkworks. It is remotely controlled by a computer, and can hover over high threat areas whilst being invisible to detection. At \$10 million it would have provided an affordable, near real time, continuous, all weather, wide area surveillance in support of tactical commanders. It can fly at an altitude of 45,000 feet, and could hover over a target area 500 miles from its launch site for eight hours, evading detection and defence with its low observable design. The Department of Defence cancelled the Dark Star UAV program in February 1999 due to budget cuts. Given a trade-off between stealth and range, the Air Force chose the range of the non stealthy Global Hawk over Darkstar's stealth [11].



Figure 2.2.4.1 DarkStar [4]

2.2.5 The Hoverbot

Of all the UAVs investigated the Hoverbot was the most informative as it was closely linked to the group's current design and it exhibited the same budgetary constraints. The Hoverbot was the result of similar University project to this one, carried out by the University of Michigan.

The Hoverbot had four rotor heads and four electric motors to complement them. It also comprised of eight sensors for control, these included; three gyros primarily used to measure the rate of rotation about the roll, pitch and yaw axes and control the damping. Three accelerometers to measure accelerations in the x, y, and z directions, and were used for the overall control. One ultrasonic sensor for close proximity height sensing, to an accuracy of a few millimetres, and one fluxgate compass for heading information to $\pm 0.5^\circ$. The fluxgate compass could not replace the gyro θ because of its slow sampling time e.g. in the order of 0.4 seconds [12].

The design of the Hoverbot led to understanding of the current platform in the sense of rotor or ducted fan position. I.e. "the distributed weight of the 4 rotor heads increases the moment of inertia and thereby the time constant of the system" [12] this in turn enables more time to sense changes and correct them, hence explains the current position of the ducted fans in the current platform design.

This design also gave an insight into how the current platform can be controlled. Figure 2.2.5.1.a shows that increasing two adjacent fans will cause the platform to tilt and create a thrust component perpendicular to side that was raised.

Figure 2.2.5.1.b shows that by having counter rotating fans the platform should stabilise itself with respect to yaw, which is the horizontal rotation of the platform. Although this will only hold true if the moment induced on each fan is the same, as the reactive force of the blades against air must cancel each other. By using this information the platform can be forced to rotate right or left depending on which pair is increased.

The height control of the platform can be achieved by collectively increasing or decreasing the power to all four motors in normal operation, or by increasing or decreasing opposite pairs when performing horizontal rotation.

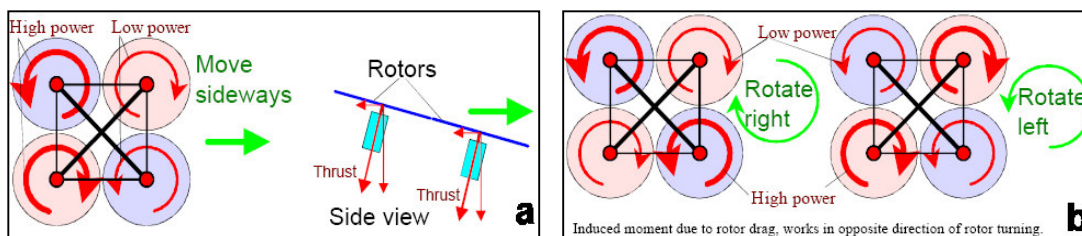


Figure 2.2.5.1. Controlling the Hoverbot [12]

The Hoverbot also touched on control issues that may be useful for controlling the current platform. For instance the main control block or Multiple Input Multiple Output (MIMO) where all the sensor information is fed and then manipulated in such a way that it can control the motors accordingly, [12] states that for complete control and stabilisation, each output must be affected by all inputs. This may be implemented by the use of complex compensation algorithms.

The actual control of the Hoverbot was never implemented and tested fully. A prototype was built, but soon after funding ran out and they were forced to stop the project.

2.3 Conclusions of UAVs to Date

As can be seen from Section 2.2 it is clear that the possibility of being able to develop a fully autonomous flying platform is feasible, though it generally requires vast amounts of money and expertise. This research demonstrated that the main aspects to consider whilst designing flying platforms are issues of control, structure and propulsion.

Control can be broken into two discrete sections, height and stability. The height control manipulates the vertical motion of the platform, it is the simplest to implement and can be achieved by the use of several different methods. Such methods include the use of accelerometers, ultrasonic sensors and GPS etc.

The stability control will affect the platforms ability to stay level, manoeuvre, and stay airborne. It is normally very difficult to achieve and requires accurate sensors such as gyros, complex compensation algorithms, and complex electronic circuitry.

The structural design is very important. It has to be as light as possible whilst still maintain structural integrity during flights. It also dramatically affects the stability of the platform as it dictates the majority of constants in the control algorithms. The most common type of failures associated with flying platforms are due to inadequate stability control [9].

The propulsion system of a platform must also take great priority. It is generally the heaviest component of a platform and dictates how the platform is controlled. There are several options for propulsion systems; current designs include Internal Combustion (IC) engines, gas turbines, and electric motors. By making a choice on the drive part of the system you must also remember to incorporate the drive necessities e.g. nitro methane fuel or battery cells etc.

2.4 Analysis of Previous Groups' Efforts

It was evident from reading the 2003 reports, that the main issues they covered were the stability control, structural design, and propulsion aspects of the platform. They achieved a lot in the time given. They fully designed and constructed their structure and control circuitry. They also researched, ordered, and incorporated five ducted fans into their structure. They managed to test the stability control in one axis with relative success, and performed several tethered flights.

However, their control circuitry was prone to excessive drift, and the sensors they used were constantly failing. They did not perform complete autonomous flight. As they could not source a power supply light enough to go on the platform and powerful enough to power the ducted fans. As a result they used very large and heavy batteries and attached them to the platform via an umbilical cord.

Several recommendations were formed by the group members and these include [13]:

- Implementation of Digital control – to reduce the control system to just sensors, processor and fan motors, allowing flexibility and change of control values.
- Use an Inertial Measurement Unit (IMU) – to replace all the current unreliable sensors.
- Develop control theory in parallel with physical improvements.
- PID and PD improvement – in the area of matching and varying time constants.
- Widen operation amplifier operating regions – to gain a more accurate and responsive voltage range.
- Consider counter rotating fans – to reduce yaw effects.
- Consider anhedral design or design for effective mass distribution – to create inherent stability.
- Research new battery technology – to drive current electric motors.
- Investigate applications of current power sources – to determine if there is another way to obtain the power required to drive the electrical control fans.

This information when coupled with the research into UAVs and discussions with all the group members and project supervisors helped form the product design specification (PDS). More detail on the PDS is discussed in Section 3.1.

3 Project Management

Project management has evolved in order to plan, coordinate and control the complex and diverse activities of modern industrial and commercial projects. Its purpose is to foresee or predict as many of the dangers and problems as possible and to plan, organise and control activities so that the project is completed as successfully as possible in spite of all the risks. Project management starts before any resources are committed, and must continue until all work is finished. “The aim is for the final result to satisfy the project sponsor, within the promised timescale and without using more money and other resources than those that were originally set or budgeted” [14].

3.1 Product Design Specification (PDS)

The end result of a project must be fit for the purpose for which it was intended. Therefore it is important to define exactly what was expected of the group from the onset of project. At the beginning of the project an initial PDS was formed [Appendix 1]. This document was important as it dictated the initial organisation of the group and its set of objectives.

Although this PDS listed what was expected from the project, it was subject to change provided the changes made were justified with relevant information. An example of this was the initial concepts of batteries. It was disregarded as there are none currently available which have the required power to weight ratio necessary for platform use.

3.2 Initial Group Structure

Initially it was decided that within the group there must three fixed positions. These positions consisted of:

- Chairman – to conduct and chair meetings, and to ensure that deadlines were set and met each week.
- Treasurer – to ensure that all moneys spent on the project were properly budgeted and accounted for. Also to make sure that the project supervisors were consulted before any large purchases are made.
- Secretary – to accurately minute each meeting so that there is a record of the discussions and deadlines covered. These minutes would then be used for future reference and to resolve any disputes.

These positions were set throughout the whole duration of the project so that continuity existed. The position of Chairman was allocated to Liam Dushynsky, Treasurer to Kevin Lewis, and Secretary to James Mackenzie-Burrows.

After this initial allocation the group structure took the form of Figure 3.2.1. This structure resembles a project team organisation structure as it consisted of a team that has been specially assembled for the specific purpose. The project manager is in direct command, with complete authority for directing the participants so that the project meets all the objectives [15].

This structure is also flat which is ideal for communication throughout the group, but it does have its drawbacks, the main one being that the project manager needs to be able to understand how all the various participants operate, and to appreciate at least in outline their particular skills, working methods, problems and weaknesses. This demands a fairly wide degree of general experience.

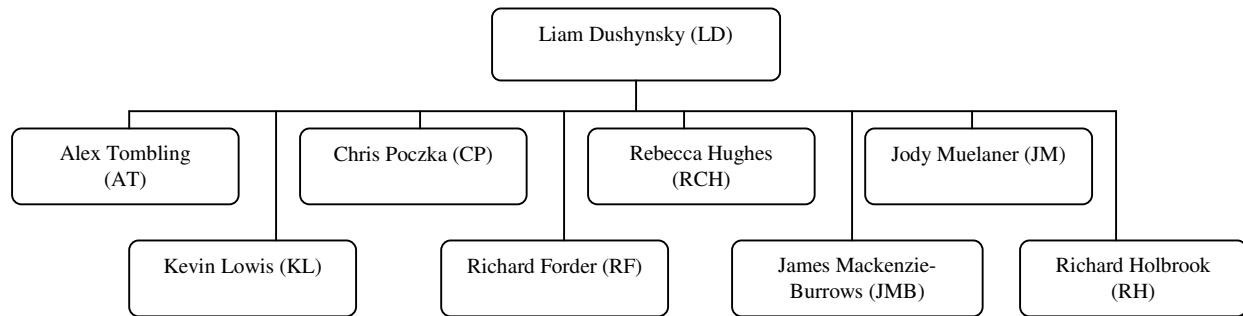


Figure 3.2.1. Initial Group Structure

3.3 Group Organisation

It is obvious that if all the project objectives are to be achieved, the people, communications, jobs and resources must be properly organised. But the form which this organisation should take might not be so obvious. Effective organisation will ensure that clear lines of authority exist, and that every member of the project knows what he or she must do to make the project a success. This was the goal of the management throughout this project.

After the initial group structure had been decided upon, the way in which the group would operate had to be confirmed.

3.3.1 Meetings

There was a group decision on structure and times of the meetings. It was decided that unofficial group meetings would be held every Monday at 10am, so that the progress over the weekend could be discussed, and official meetings with supervisors would be held every Thursday. The meeting times were chosen as to not conflict with any of the group members timetables, and it allowed for certain rooms to be booked for the duration of the project at those set times. The meetings followed a consistent structure. This structure can be seen in [Appendix 2].

Meeting agendas were made available to each of the group members and supervisors prior to every meeting. As can be seen from [Appendix 2] the agenda consisted of numbered sections that were relevant to that particular meeting and date, e.g. 30/10 6.3, referred to the 30th October, the 6th meeting, section 3 which is the Chairman's report. This was done so that the minutes could match up to the meeting.

The minutes of the meeting served several purposes throughout the duration of the project. They displayed a list of attendance, which was used to check when certain members of the group were absent. They were a record of when ideas and concepts were first discussed and they illustrated any problems that group members were having at any particular time. They also listed all the tasks that were set during the meeting or that were already pending. This was so that group members could check their records in their log books and compare it to what was actually noted so that any confusion could be rectified before the next meeting. A copy of the minutes can be seen in [Appendix 3]. Like the agendas they were made available to all members of the group prior to the meeting.

3.3.2 Section Allocation

For the group to work effectively as possible, areas of work were not initially set by any one person. The group as a whole reviewed all of the previous year's reports and concluded which sections they believed they would like to pursue. By doing this all members actively took responsibility for their particular sections, and there was no cause for resentment within the group.

This section allocation was susceptible to change throughout the duration of the project. There were numerous reasons for the possibility of change the main one being a realignment of resources as to ensure that critical tasks were met.

3.3.3 Communication

Efficient organisation and communication is essential for motivating all the group members. A well-motivated group can be a joy to work with and will generally produce good results. Whereas a badly informed group, with vague responsibilities and ambiguous levels of status and authority, is likely to be poorly motivated, slow to achieve results, and extremely frustrating to work with.

The prerequisite of good management communications is the provision of adequate feedback paths through and across the group. This allows progress to be monitored, difficulties to be reported back to the project manager and advice to be given on any problems that arise.

Communication was achieved by several different means throughout the duration of the project. The most obvious was at group meetings where all group members were present, and discussions of problems, current progress, and expectations could be carried out. Another method of communication was via the internet which allowed for communication of information over weekends and other periods of time where contact between members was difficult. The last and probably most effective method of communication was the introduction of core time. Core time was set in place to make sure that all members of the group were on the university campus at set periods of time. These times were set at 11am-1pm every Tuesday, Wednesday and Thursday, although each week did vary depending on the current circumstances. This enabled group members to ascertain information from other group members almost instantly. The lab in which the group worked in had a white board which was dedicated to this time. The in-out board can be seen in Figure 3.3.3.1. This was used to show where all the group members were during core time. It was found to be so effective that it was commonly used at other times as well.

NAME	IN	OUT
ALEX	LAB	
BEX	207	
CHRIS	CAD/CAM	
JAMES	LAB	
KEV	K-LAB	
LIAM	K-LAB	
RICH F.	K-LAB	
RICO	207	
JODY		✓

CONTROL/IMU:
KL, RH, RF, AT, LD

PROPULSION:
RH, JME, AT, CP, LD

GENSET/ELECTRICAL POWER SYSTEMS:
AT, SMB, RH, LD

STRUCTURE:
CP, RH

Figure 3.3.3.1. In-Out Board

3.3.4 Information

Information exchange is a result of communication. For the group to be effective information had to be shared with ease. There were several ways in which the group did this. The main method was by handouts at group meetings, this was usually done when a group member was explaining his or her work within the meeting. Another method was by WebCT.

WebCT is a program designed by Exeter University and its role is to act as an information storage site on the internet that can be accessed from anywhere, providing the right username and password are inserted. WebCT is where the minutes and agendas for each meeting were stored. Folders were also set up that covered different aspects of the project, these folders could then be added to by posting information into them. For instance, all project management files that were created by the chairman were put into the project management folder. This could be accessed by any of the group members from any location, which allowed them to review the project status whenever they wanted to without seeking consultation from the chairman. Once WebCT was up and running, a file was created that listed the last five updates. This was done to save time in searching for newly uploaded files through all the various folders. Screen shots of WebCT can be seen in [Appendix 4, Figures 4.1 and 4.2].

The last method used to display information was the use of the whiteboards and walls in the workshop. The white boards were used for either teaching purposes between group members or for keeping other members informed of the current situation, i.e. pending tasks. The walls were used to display project management information. Large versions of the Project analysis, in the form of Gantt Charts, Tracking Gantts, and Network diagrams were printed out and attached to the wall for all group members to see and relate to. More information on the Project analysis can be seen in Section 3.4. An example of this method can be seen in Figure 3.3.4.1.

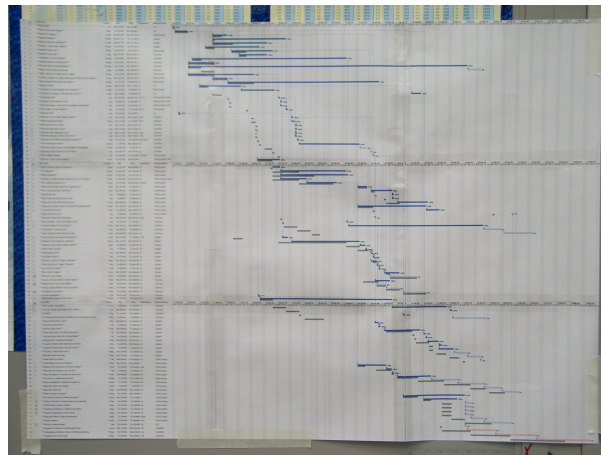


Figure 3.3.4.1. Tracking Gantt displayed on the workshop wall

3.4 Project Analysis

The need for project planning has always been present in project coordination. Ideally strategic plans are made before the start of an operation and by following them; the operation is successfully concluded [16]. However this is not the case as operations rarely go according to plan. This was evident within the early stages of “The Design and Development of the Flying Platform” project.

3.4.1 Initialisation of the Project Plan

After the initial group structure was formed and the PDS was specified. The group collaboratively made suggestions on what was believed to be the course of action for the project and what tasks may be involved in carrying out these actions. The results of this initial brainstorming session were collaborated and are depicted in [Appendix 5 Figure 5.1]. This initial depiction of the project was good in the sense that an overall understanding of the project was obtained, but it lacked in terms action order. Therefore a flow chart of this initial overview was constructed and can be seen in [Appendix 5 Figure 5.2].

After the flow of the project was determined, it was suggested that each group member should have an individual flow chart to illustrate what they would do. This idea was abandoned as the group members believed that this was an inefficient use of time, as their objectives would be likely to change and therefore making the flowchart useless. An example of the proposed individual flow chart can be seen in [Appendix 5 Figure 5.3].

3.4.2 Planning and Scheduling Methods

The flow chart of the initial overview as shown in [Appendix 5 Figure 5.2] formed the basic project plan. For this plan to be useful it had to be manipulated in such a way that timescales could be added and the interrelationships between all the tasks could be seen with ease. This led to the investigation of several planning and scheduling methods. The main methods investigated were Gantt Charts and Network Analysis.

3.4.2.1 Gantt Charts

Named after Henry Gantt (1861-1919) [17], these charts are represented by bars that are drawn or constructed on a scale where the horizontal axis is directly proportional to time. They can be used to show logical progression of tasks by the addition of arrows. They have the advantage that they are simple to draw and read, good for static environments, and useful for providing an overview of project activities. They also have the disadvantage of being difficult to update manually when there are many changes, they can quickly become obsolete and therefore are discredited, they do not equate time with cost, and they do not help with optimising resource allocation [18].

3.4.2.2 Network Analysis

Network analysis is a generic term for several project planning methods which can be traced back to developments in Europe and elsewhere, but their full exploitation was seen in the late 1950s, when they were used with great success and much publicity for the planning and control of US defence projects [17]. They are now commonly found throughout companies around the world. Networks are weak in their ability to set out tasks on a time-scale although they do have the advantage of being able to provide the more powerful notation needed to show all the logical interdependencies between different tasks. They also allow priorities to be quantified based on an analysis of all the task duration estimates. Those tasks that cannot be delayed without endangering the project completion time are identified as critical, and all other tasks can be ranked according to their degree of criticality [19]. The types of Networks systems considered were the arrow networks, these include:

- Arrow Diagrams (ADM)
- Critical Path Analysis (CPA)

- Programme Evaluation and Review Technique (PERT)

3.4.2.3 Software Packages

Before a decision could be made on which planning and scheduling method to choose, there had to be an investigation of the software packages that were available. The cost of the software, its functional abilities, and ease of use were all determining factors. The main software products considered are listed below:

- eTaskMaker [18]
- Plan for Windows [21]
- Project Kick Start [22]
- WBS Chart Pro [23]
- PERT Chart Expert [23]
- Microsoft Project [24]

3.4.2.4 Method Choice and Reasoning

Whilst considering all the factors in the preceding sections, it was decided that the project analysis methods to be used were; Gantt Charts, Tracking Gantt and Network Diagrams. This was so that the initial project plan could have a time scale and could be clearly seen by the use of a Gantt chart. Then any progress or modifications could be made and then seen by the use of a Tracking Gantt. Then the Network Diagrams would be able to show all interrelationships between the activities and display their start and finish dates. Thus by using all these methods all aspects vital for good project planning and scheduling would be covered.

The software program used to carryout this project analysis was Microsoft Project 2003, as it has the ability to perform all the functions necessary and no duplication of data is necessary. This is possible as it can use the same information for each of the three methods. Added advantages are that it is relatively easy to manoeuvre between methods, critical paths can be added, it is free, and it is relatively easy to use.

3.4.3 Planning and Scheduling

After the flow chart of the initial overview was constructed and the planning and scheduling techniques were decided, an initial Gantt chart was constructed as can be seen in [Appendix 5 Figure 5.4]. This Gantt chart was displayed to the rest of the group and altered accordingly subject to any inaccuracies. A baseline was set so that any alterations made in the future could update the chart without erasing the old version.

Once the first chart was agreed on, it was displayed in the workshop and on WebCT along with the current Network diagram. An example of the displayed Network diagrams can be seen in [Appendix 5 Figure 5.5]. By displaying the information in this way it allowed all members of the group to study the projects progress at any time. The Gantt chart was then subsequently updated at a periodic rate of one month and displayed in the form of a Tracking Gantt. The Tracking Gantt showed the current situation compared to the initial planned progress see [Appendix 5 Figure 5.6].

For this method of planning and scheduling to be effective, it relied on constant communication and feedback from the group members. For the first few versions of the Project analysis, it was found that group members did not actively check the project plan and feedback any information as a consequence. This was believed to be due to the nature of the charts not being easy to scan for particular tasks. Therefore resources i.e.

discipline's of the project, were allocated to tasks. This was achieved by labelling the bars in the Tracking Gantt and colour coding the Network diagrams accordingly. Also a breakdown of the tasks was performed and a list of each disciplines tasks were given to the relevant members of the group. This aided the feedback process and helped in creating a more accurate project overview. The data that went into the last Project Analysis can be seen in [Appendix 5, Figure 7, parts 1 & 2).

3.4.3.1 The Management of Change

It was soon realised at the beginning to the project that deadlines and tasks were likely to change, therefore it was the job of the project manager to be constantly aware of any obstacles that may arise. This involved the constant monitoring of the progress of each task and was aided by allocating other members of the group as chairmen of particular sections, see Section 3.5. This enabled responsibility to be shared and efficiency to be increased, as the chairmen of particular groups would be able to set more reasonable deadlines, create new tasks and dismiss wasteful activities. By having these chairmen the group as a whole communicated better and group meetings were more effective as smaller issues were resolved within the subgroups.

3.5 Revised Group Structure

As discussed in the preceding section the group was segregated and overall responsibility was shared. There were four distinct groups or disciplines; Control /IMU, Propulsion, Electrical Power Systems, and Platform Structure. These groups each had their own section within the meetings as can be seen in the Agendas and Minutes [Appendices 2 and 3]. Figure 3.5.1 shows the new group structure and the members within each group.

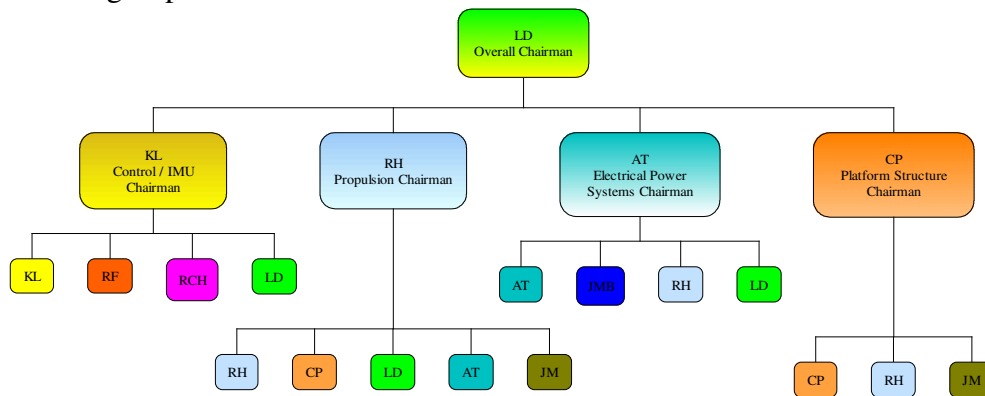


Figure 3.5.1. Revised Group Structure

Although this predominantly takes the appearance of a hierarchical structure, or matrix organisation, it still maintained the practice of a flat structure with constant horizontal communication between the subgroups.

3.6 Conclusions

The four main stages of the project planning process were completed successfully. These include; identifying the constituent activities, determine their logical sequence, prepare estimates of time and resource, and present the plan in a readily intelligible format.

Despite the structure of the project analysis being well implemented, several deadlines were not met and the project fell behind schedule. This is believed to be a result of many factors.

One factor that was evident was the group's perceptions of deadlines. For if a project is to succeed, the actual progress will have to match or beat planned progress. The majority of the tasks were only fully attempted just before the set deadlines as a last minute effort. If difficulties occurred, there was no time to overcome them before the deadline, and the tasks would fall behind schedule. As the majority of the tasks were linked, it also resulted in putting all the preceding tasks behind schedule. This only had to happen a few times before the project got into a state that was hard to get on track.

Another factor was optimistic and deliberately misleading information that skewed forecasts of time and perceptions of performance. It is a common trait of manufacturing firms to quote figures that are only obtainable in highly controlled environments and then giving the perception that the same results are obtainable by the public with ease. The result of the group being gullible in certain situations caused initial plans to be recalibrated which took unexpected time and caused excessive delays.

The most common factors that caused the project to fall behind schedule found throughout the duration of the project were the failure of mechanic parts, excessive time spent debugging circuitry, and other module commitments.

After being involved with the management of the project, several realisations were made. The first realisation was that there is more to the practice of effective project management than the application of a few sophisticated computer programs. It embodies a framework of logical and progressive management, perceptiveness, the application of common sense and proper organisation. The second is that no matter how experienced, competent, enthusiastic and intelligent the person chosen for the job of project manager, he or she cannot expect to operate efficiently alone, without adequate support and cooperation. This obviously includes the willingness and cooperation of all the members engaged on the project

3.7 Recommendations

There are several recommendations that are to be made. The first is to start the project as soon as possible, and for all members to have a clear perception of the problems at hand by reviewing the previous work done intricately. The second would be to limit the level of detail in the project analysis. This can be achieved by grouping certain aspects of the project together, as vast task lists can seem daunting and can deter group members from reviewing it.

Setting deadlines, it would be beneficial to illustrate the point that deadlines are the latest possible finish date and that all members should strive to complete work before the deadline, and then actively seek further work. It would also be advisable for the project manager to motivate each group member according to their personality, which in some instances maybe by gentle persuasion and others by inducing fear and trepidation.

But above all to be aware that the average participant will appreciate being led by a project manager who displays competence, makes clear decisions, gives precise, achievable instructions, delegates well, listens to and accepts sound advice, is enthusiastic and confident, and thus generally commands respect by example and qualities of leadership.

4 Propulsion

There were four areas that were investigated within the propulsion system these include, Perimeter Fans, Central Fan, Duct Design, and Personalised Fan Design and Construction

4.1 Perimeter Fans

These fans were purchased by the previous group in 2003. The main function of these fans was to stabilise the platform. There were several components involved in making these fans run, these include; a Plettenberg HP220/20/A4 F P4 electric motor, a Schulze Future 32.55 speed controller, and a WeMoTec Midi Ducted Fan. Details on the operation of these fans operate can be found in [25]. Initial testing was performed using a PC which enabled a pulse width to be generated, which was fed into the speed controllers [25], although this method was prone to error it did produce approximately the same results as the previous year, i.e. that they can produce maximum thrust is just over 2 kg. A detailed analysis of all the results can be found in [26]. This thrust limit meant that they could only produce approximately 1-1.5 Kg of thrust each for the height of the platform e.g. 4-6 Kg, whilst still being responsive enough to control the stability of the platform. As a result of this more thrust must be required from the central fan.

4.2 Central Fan

This year's central fan design was governed by the PDS. It had to incorporate an IC engine which may eventually double as a power generator. Research was carried out on the best options for IC engine and fan combinations [27], the best option currently available that was within the projects budget was range was an OS91 VR-DF large head, with the Ramtec 5 ¼ inch ducted fan unit [27]. This combination on paper was believed to provide the necessary thrust to raise the platform i.e. 6 Kg [27]. As this engine and fan combination would come from the US it was decided that a spare of each should be ordered in case of failure, as a result of the long lead times expected.

4.2.1 Run-In

When the engines arrived they had to be “run-in”, this was done by following the instructions supplied with the engine, see [Appendix 6], although a 10” propeller was used from the onset instead of a 12” propeller, due to unavailability, and discussion with Dr M.A. Jenkins concluded that this would still be ok to use. The rig in which the engine was held for this “run-in” can be seen in Figure 4.2.1.1, and its design and construction can be found in [27]. Once the engine had been “run-in” with the propeller it needed to be “run-in” with the ducted fan unit as the instruction state it should be “run-in under the same conditions as when put to full use” [Appendix 6], therefore the fan unit was constructed and attached to the engine [27] see Figure 4.2.1.2.

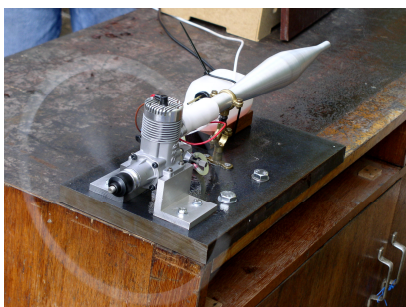


Figure 4.2.1.1. Propeller “Run-in” Setup

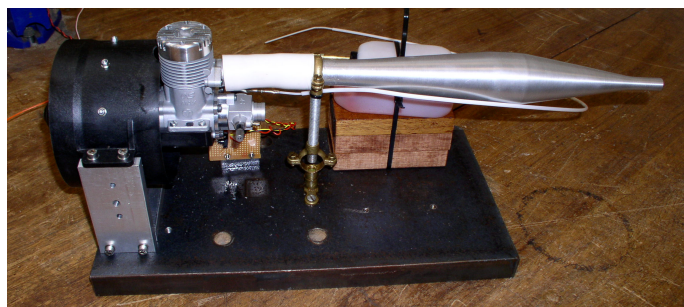


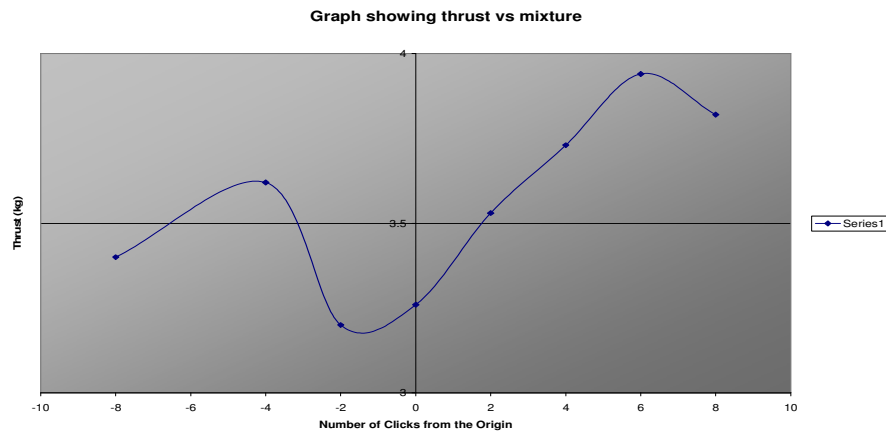
Figure 4.2.1.2. Ducted Fan “Run-in” Setup

4.2.2 Testing

After run-in had been completed the engine was mounted into a vertical position on a new rig, this new rig was adaptation of the previous years test rig. The design and construction of this rig can be found in [27]. The rig exhibited a “see-saw” action which enabled a set of scales to be placed at one end, which in turn would measure the exact thrust from the engine. This was possible as the moments about the centre were made the same by the addition of a counter weight.

Initial testing was done to see how many revolutions per minute (RPM) there were being generated from the engine; this was done by the use of strobe which was held over the fan unit as it was running. This proved that the engine was not running out of the specified limits. After the initial testing was done, thrust readings were taken and matched to RPM values, these can be found in [27]. The next set of tests involved changing fuel mixtures; this was done in two ways. The first way was to increase the nitro content of the fuel, which in theory should increase the performance, at the expense of decreasing the engines life. The second way is to change the needle valve settings, which alters the fuel to air ratio, causing the engine to run either “richer” i.e. more fuel less air, or “leaner” i.e. less fuel more air.

Initially the fuel was 10% nitro, this was then changed for 16% nitro and tested under the same conditions. The results concluded that the change in performance was not significant enough to be conclusive that the fuel mixes make any difference [Appendix 7]. Further information on the analysis of this can be found in [27]. The needle valve was set by the manufacturers at a specific point that would be optimal for engine “run-in” i.e. slightly “rich”. This setting was adjusted by 2, 4 and 8 clicks in both the clockwise and anticlockwise directions. This unlike the change in mixes did cause a significant difference. The results of this test can be found in Graph 4.2.2.1 [Appendix 7].



Graph 4.2.2.1. Effect of Changing the Fuel to Air Ratio

4.2.3 Conclusion

The conclusion of this initial testing with the ducted fan was that the manufactures were wrong in their estimates, as only a maximum of 4.1 Kg was ever achieved. Therefore another method of increasing the thrust from this fan was required or alternatively a completely new IC and fan combination. This led to the investigation of duct design.

4.3 Duct Design

In theory by channelling the airflow into and out of the fan correctly the performance should be increased. This should happen as there is less interference with linear flow. More information on the theory behind duct design can be seen in [27] and [28].

4.3.1 Duct Construction

The ducts used in the testing were made of thick card and were held together by duct tape. The design and construction of these ducts can be found in [28]. In total there were several designs, which include both top and bottom ducts. The five main top ducts that were used in testing can be seen in Figure 4.3.1.1. The numbering of these ducts goes from 5-1, from left to right respectively.

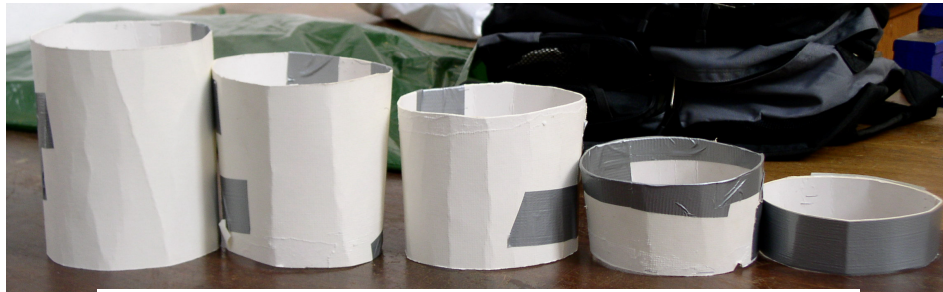


Figure 4.3.1.1. Different Top Ducts

Two different bottom ducts were made, one in which the area throughout the duct was attempted to be maintained and the other where the area became bigger.

4.3.2 Duct Testing

The ducts were secured onto the current ducted unit by duct tape. Different combinations of the ducts were tested, it was found that the bottom ducts decreased the average thrust substantially and the top ducts increased the thrust characteristics. The best result obtained was with duct 4 alone, this gave a thrust of 5.1 Kg. Figures 4.3.2.1 and 4.3.2.2 illustrates the duct testing setup. Further information on the results of the duct testing can be found in [Appendix 7] [27] [28].



Figure 4.3.2.1. Combination of Ducts

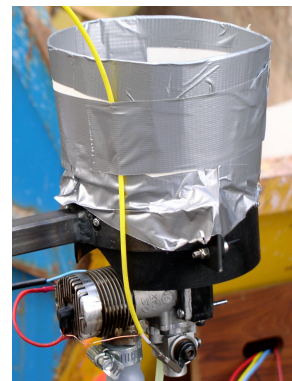


Figure 4.3.2.2. Top Duct Alone

4.3.3 Conclusion

The top ducts increased the performance up to a certain height, but the performance increase has to be greater than the weight of the duct. This testing also proved the bottom ducts to be detrimental, and indicated that they should not be used. I would suggest that

proper ducts are made, to precise measurements and then tested before a final conclusion can be reached on which height is optimum.

4.4 Personalised Fan

It was believed that the current fan constructions on the market are not as efficient as possible; therefore a dedicated member of the group devoted all their resources to designing and simulating a fan design which would greatly increase the performance from the same engine currently used. More information on the design, simulation and possible construction methods can be found in [29].

4.4.1 Conclusion

Currently the full details of this design have not been disclosed; therefore for further information see [29].

4.5 Problems Involved with Propulsion Testing

The vibrations of the engine caused many problems. It resulted in many mechanical failures of the structure, examples include; screws shearing off, cracks appearing and propagating, hex bolts loosening, glow-plugs braking and loosening and many more. Some of these failures can be seen in Figure 4.5.1.

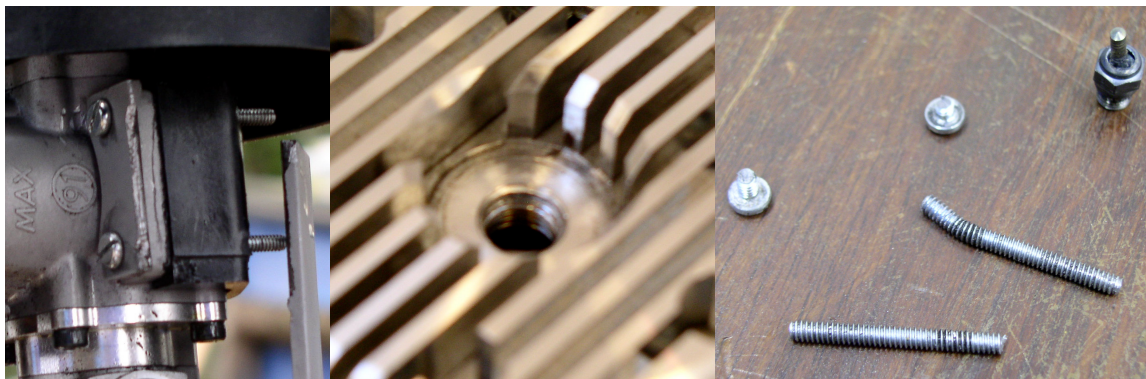


Figure 4.5.1. Component Failures

The result of all these component failures was that much more time than anticipated was spent achieving trivial test results. This coupled with the testing time restrictions placed on the group, forced the progress to fall far behind schedule.

4.6 Overall Propulsion Conclusion

After performing the tests on the IC engine and perimeter fans, it was evident that there would not be enough lift generated to raise the platform. It also demonstrated that controlling the IC engine accurately, would be a near impossible task as it constantly “hunts”, i.e. the RPM of the engine never stayed constant. Therefore it was hard to determine which solution would be best. I believe the best cause of action would be to pursue with the top ducts and alter the fuel settings so that maximum thrust is gained. Failing that I would suggest the investigation of Gas Turbine engines as the power the weight ratio far exceeds that of any IC engine, for more details on Gas Turbines see [27].

5 Control

The control system is necessary to stabilise the platform and control the height at which the platform must fly. Height and stability control were investigated as they form part of the performance requirements in the initial PDS.

The control of the platform was split into four discrete sections. These sections are illustrated in Figure 5.1. The sensors have to be able to provide information on the platform's attitude and displacement. The control signals are manipulated signals from the sensors. These signals can be fed into the control implementation process. The control theory dictates the way in which the control signals must be used in order to give the desired effect on the physical system i.e. the platform.

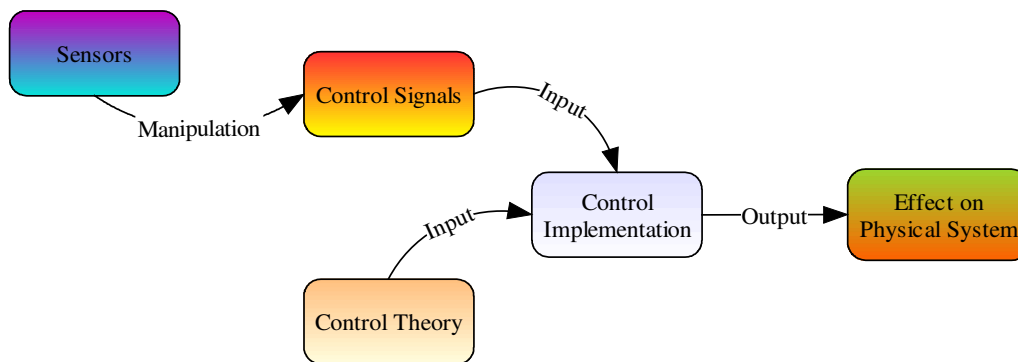


Figure 5.1. Control Structure

This report investigates the sensors involved in the control system and the way in which the signals were manipulated to give the desired output for the control implementation.

The following sections refer to the right-handed axis set, where Roll is defined by rotation about the x-axis, Pitch about the y-axis, and Yaw about the z-axis. This system can be seen in Figure 5.2.

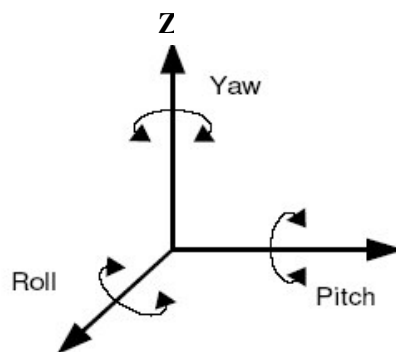


Figure 5.2. Right-handed Axis Set

5.1 Sensor Research

In order for the control system to be able to monitor and consequently change the movements of the platform, a number of sensors were required. Research was performed into the various sensor and sensor systems that may be applicable for the control system and these are detailed below.

5.1.1 Accelerometers

Accelerometers are sensors and instruments for measuring, displaying and analyzing acceleration and vibration [30]. They measure the inertia force generated when a mass is affected by a change in velocity. They are composed of three main elements, a mass, a suspension mechanism, and a sensing element that returns an observation proportional to the acceleration of the mass [31].

Accelerometers can have from one axis to three axes of measurement, the multiple axes typically being orthogonal to each other [32]. These devices work on many operating principles. The most common types of accelerometers are piezoelectric, capacitance, null-balance, strain gauge, resonance, piezoresistive and magnetic induction.

As accelerometers measure acceleration in one or more axis, they can also be used to measure displacement, as displacement is the double integral of acceleration over time according to calculus, as shown in Equations 1 and 2 [33].

$$v(t) = \int_0^t a \, dt + C \quad (1)$$

$$r(t) = \int_0^t v \, dt + D \quad (2)$$

Where:

a = acceleration of a mass

v = velocity of a mass

r = displacement of a mass

C and D = constants of integration

Three main features must be considered when selecting accelerometers are amplitude range, frequency range, and ambient conditions. Acceleration amplitude range is measured in Gs (9.81m/s^2), whereas frequency is measured in Hz. For the ambient conditions, such things as temperature should be considered, as well as the maximum shock and vibration the accelerometers will be able to handle. This is the rating of how much abuse the device can stand before it stops performing, which is entirely different from how much vibration or acceleration accelerometers can measure.

5.1.2 Gyroscopes

Gyro sensors are commonly used for angular measurement. The output of a gyro is proportional to the rotation velocity that it is subject to. There are several types of gyros

currently available on the market they all vary in accuracy and price. The most widely used are Micro Electro Mechanical Systems (MEMS) gyros, e.g. a revenue of \$279 million in 2002 and an expected revenue of \$396 million in 2007 [34]. MEMS sensors measure angular rate using the Coriolis force.

It is important to note that a rate sensor cannot measure an angle or orientation by itself. It only measures rotational motion. To obtain the angle, the angular rate has to be integrated over time, which in turn gives an angle as a function of time. This can be seen in Equation (3) [35].

$$\theta(t) = \int_0^t \omega(t) dt + D \quad (3)$$

Where:

θ = angle of which the mass has rotated

ω = angular velocity at which the mass is rotating

D = integration constant

The main features to be considered when selecting angular rate gyros are the scale factor and drift. The scale factor describes the capability of the gyro to accurately sense angular velocity at different angular rates. Gyro drift characterises the ability of the gyro to reference all rate measurements to the nominal zero rate output.

5.1.3 Inertial Measurement Units

An inertial measurement unit is a complete six degree of freedom measurement system that consists of an internal sensor array of rate gyros and accelerometers, usually three of each, that enable it to provide rotational rate and acceleration about the x, y, and z axis. Most inertial measurement units are constructed in “strap-down” configuration, which means that the gyros and accelerometers are normally fixed to a common chassis and are not actively controlled on gimbals to align themselves in a pre-specified direction. This design has the advantage of eliminating all moving parts and is inherently more reliable [31]. Inertial measurement units will provide the range of outputs required to perform platform control, they are commercially available but are also high in price e.g. Omin Instruments MT9 is £1125 [36]

5.1.4 Horizontal Auto-Levelling Device (HALs)

These devices are used within model aircraft control systems. They basically simulate an artificial horizon by outputting a voltage corresponding to the amount of light hitting a light detecting diode, which is positioned on a free moving gimbal. These devices were not investigated fully as it was clear that there are none accurate and fast enough for the purposes of a flying platform.

5.1.5 Fluxgate Compass

A Fluxgate compass is a magnetic heading sensor generally used for pleasure craft and coastal fishing. Some new fluxgates like PG-500 consists of a fluxgate sensor, solid-state rate gyroscope, processor and serial data interfaces. “The sensor detects the heading relative to the magnetic north as induced within the fluxgate coils by terrestrial

magnetism” [37]. Fluxgates can be very accurate and are good for determining the average heading, but as discussed in Section 2.2.5 they are not responsive enough for determining the actual angle at any given time.

5.1.6 Ultra Sonic Sensors

Ultrasonic transducers are used as range sensors for map building and collision detection in autonomous guided vehicle (AGV) applications [31]. They typically use the speed of sound to determine distance. As the speed of sound is accurately known, the ultrasonic sensor can output a sound, and record the amount of time it takes to return. This information can then be used to determine the distance, as distance is equal to speed multiplied by time.

These will not be accurate enough for platform use due to the physics of sound propagation. The waves suffer specular reflection, diffraction, and multi-path reflection from oblique specular surfaces, and absorption by porous surfaces. This in turn will create an inaccurate interpretation of the return echo.

5.2 Sensor Choice

It was apparent from the research above and the recommendations from the previous year’s group that inertial measurement units would be the best option for the control sensors, as they provide all the necessary outputs from a single unit. They provide information on Pitch, Roll, and Yaw rotation that can be used for stability control. As well as acceleration in the x, y and z-axis that can be used for height control. But due to budgetary constraints it was believed that they would be too expensive to purchase.

However after some discussion and negotiation with BAE Systems, carried out by Dr G.A. Lester and Dr M.A. Jenkins, it was agreed that a prototype, military grade inertial measurement unit would be lent to the University. Therefore the group decided that this inertial measurement unit would be incorporated into the platforms control system. It can provide more information than currently needed, which will be advantages for future developments.

6 SiIMU0X[®] Inertial Measurement Unit

The SiIMU0X known as the IMU from now on, provides inertial measurements in terms of angular rate, angle increment, linear acceleration, and velocity increments in three orthogonal axes. It also provides inclination measurements in terms of angle from the vertical in the Roll and Pitch axes. It comprises of three silicon micro-machined gyroscopes for angular rate measurements, three silicon accelerometers for the measurements of linear acceleration, and two silicon accelerometers for the inclination measurements in Roll and Pitch. The IMU also uses the right-handed axis set, a correlation between the axis and the physical structure can be seen in Figure 6.1.

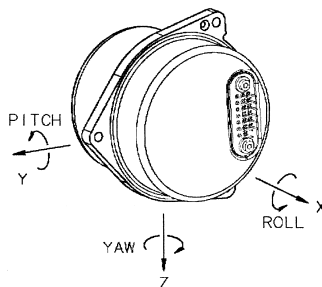


Figure 6.1. IMU Orientation with Respect to the Axes [38].

The gyros are capable of measuring $\pm 50^\circ/\text{s}$. The accelerometers can measure up to $\pm 15g$ and the inclinometers can measure $\pm 15^\circ$ in the Roll axis and $\pm 53^\circ$ in the Pitch axis [39].

6.1 IMU Interface

Measurements of the angular rates, linear accelerations, and inclinometer angles from the IMU are output as a serial digital data stream. This data is transmitted at a frequency of 50Hz. The serial data message consists of eleven, twenty-four bit serial words containing the information from the gyros, accelerometers, and inclinometers.

The interface consists of three differential pair transmission lines developed in accordance with the electrical specification of RS-422, these signals are [39]:

- Data Out
- Clock
- Sync out

The timing diagram of these signals provided by BAE systems can be seen below in Figure 6.1.1.

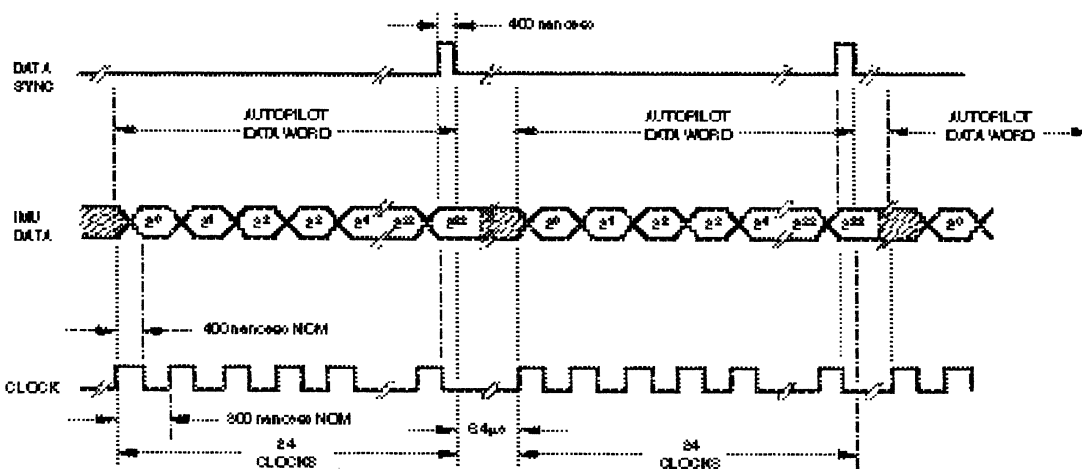


Figure 6.1.1. IMU Signal Timing Diagram [39].

A clock pulse is generated for each message bit transferred in the data stream, and a synchronisation signal is generated to mark the end of each transmitted word. Therefore to output all the necessary information a total of 264 clock pulses and 24 sync pulses are required.

6.2 Serial Data Message Breakdown

As discussed above there are eleven serial words each containing 24 bits. These 24 bits can be broken down into two fields, the Header Field and the Data Field. The Header Field is 8 bits long and contains a word identifier, Health status, and BIT status. Although the Health and BIT status were not included in the IMU we were given and therefore cannot be used.

The Data Field is 16 bits long and contains the inertial data. The inertial data is given in two's complement form which enables the information to be either positive or negative to a resolution of 15 bits (32768 levels). The first bit of each field is transmitted least significant bit (LSB) first. This word format is shown in Table 6.2.1.

Header Field								Data Field															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Identifier				Health		Bit		Data															
LSB							MSB	LSB															MSB

Table 6.2.1. Data Word Format [34].

The 23rd bit indicated by the yellow background is the two's complement part of the data field. Bits 4-7 as indicated by the red background are the bits in the header field that can be ignored.

6.2.1 Word Identifier

The word identifier consists of four bits that can either represent a one or a zero, as the signal is digital. Thus the word identifier can recognise up to 16 bits, although only 11 of these will ever be used. A description of the word assignments and transmitted order can be seen in Table 6.2.1.1.

Transmit Order	Word Identifier				Word Assignment	Decimal Value of Word Identifier
	Bit 0	Bit 1	Bit 2	Bit3	Data (16 Bits)	
1	1	0	0	1	X-Axis Acceleration, Ax	9
2	1	1	1	0	Roll Inclinator, Ri	14
3	0	1	0	1	X-Axis Gyro Rate, Gx	5
4	0	0	0	1	Pitch Inclinator, Pi	1
5	1	1	0	1	Z-Axis Acceleration, Az	13
6	0	0	0	0	Temperature Data, Temp	0
7	0	0	1	1	Y-Axis Gyro Rate, Gy	3
8	1	1	1	1	BIT Data, BIT	15
9	1	0	1	1	Y-Axis Acceleration, Ay	11
10	0	1	1	1	Z-Axis Gyro Rate, Gz	7
11	1	0	0	0	Null Word	8

Table 6.2.1.1. Word Identifier Assignment [39].

The sections highlighted in red are sections that can be ignored as they will not give out any useful information as a result of them not being implemented on the IMU as discussed earlier.

7 IMU Decoder Design

The control implementation stage of the platform design requires analogue voltages in order to feed control loops and operate effectively. The decision of why analogue control was used can be found in [40] [41] and an in depth discussion on the control implementation stage can be found in [40]. These analogue voltages also need to be available constantly. This goes for all sensors that are used in the control implementation stage. Therefore there are obvious problems with the current outputs from the IMU. They are digital and they are only available for a set period of time. Therefore in order for the IMU to be effective the signals must be manipulated in such a way that all sensor readings are made analogue and must be available constantly.

7.1 Serial to Parallel Conversion

In order to manipulate the digital signal the 24 bit serial data word has to be split up into the two constituent parts, the Header and Data Field. This will enable the sensor identity and data to be worked on concurrently for reasons that will be discussed shortly.

To do this the serial data has to be converted into parallel data. The most common method to achieve this is by using shift registers. Shift registers are comprised of a chain of flip flops where each Q output drives the next D input, and all clock inputs are driven simultaneously [42]. This enables the serial information to be shifted along one place every clock cycle, and all shift register outputs are constantly available, hence converts serial data to parallel data.

Therefore to convert the serial data word into two parallel outputs, one for each field, three 8-bit shift registers would be required, as there are 24 bits. The set-up of the three shift registers and can be seen in Figure 7.1.1.

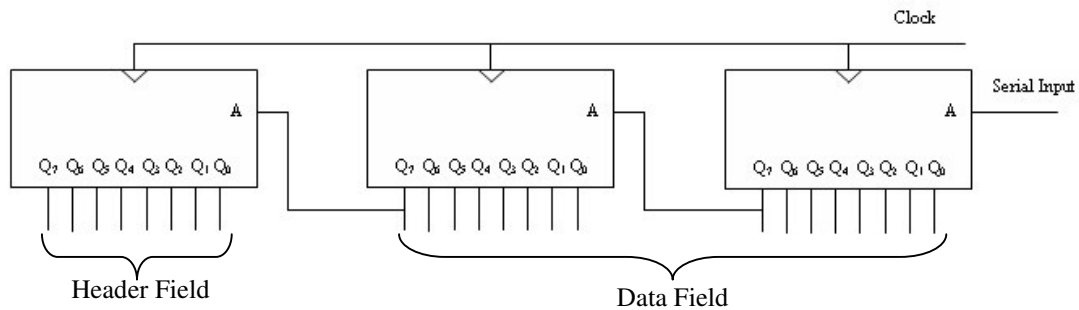


Figure 7.1.1. Shift Register Setup

Due to high availability and low price of £0.31 [43] the 74F164A manufactured by Fairchild SemiconductorTM was chosen to be the most suitable for this application. For more information on the 74F164A see [Appendix 8]

7.2 Digital to Analogue Conversion

Once the data word has been split up and the data field is available in parallel format, it needs to be converted from a digital signal to an analogue signal. The most obvious way of doing this is to use a Digital to Analogue Converter (DAC). For the purpose of a DAC is to convert a quantity specified as a binary number to a voltage or current proportional to the value of the digital input [44].

After research the DAC found to be most suitable for this purpose was the DAC712 manufactured by Burr-Brown. This was because this DAC it was relatively cheap at £17.40 [43], it is capable of receiving 16-bit parallel data in the two's complement form, and it has a quick conversion time. Other advantages are its output voltage range of $\pm 10V$ which would provide a good range of voltages depending on the input, and it has also got GAIN and OFFSET adjustments that can easily be trimmed by potentiometers. For more information on the DAC712 see [Appendix 9]

7.3 Word Identity Decoder

As discussed in Section 6.2.1 there are 4 bits in the header field that identifies which sensor the data is coming from. To be useful this identifier will have to be decoded and then used as a chip select. The simplest way to achieve this is by using a 4-16 decoder, as it takes four inputs i.e. the identifier, and outputs only one output at a time depending on the configuration of the inputs. This is illustrated in Table 6.2.1.1., where the decimal value of the identifier word will correspond to that particular output pin. See Figure 7.3.1. for a typical example with an input of 3.

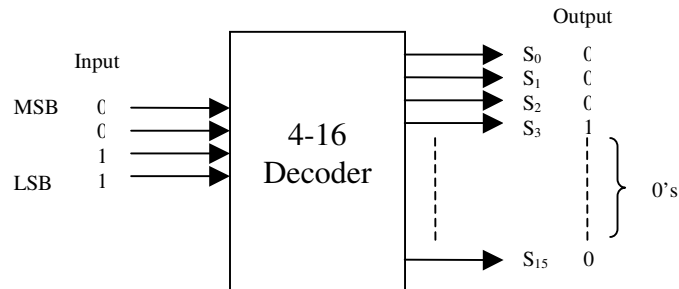


Figure 7.3.1. 4-16 Decoder Example

After investigation of current 4-16 decoders it was decided that cost should be the determining factor as they all perform the same basic function. Therefore the CD4514BCN manufactured by Fairchild Semiconductor™ at a cost of £1.02 [43] was chosen. More information on this chip can be seen in [Appendix 10].

7.4 Voltage Storage

As the sensor can now be identified whilst the data is being transformed into an analogue voltage, the next step is to consider how to store this voltage in an appropriate place. There are 8 outputs that we are concerned with as shown in Table 6.2.1.1., therefore there must be a minimum of 8 storage devices. After initial research with R. Forder and discussions with M. Horwood and Dr G.A. Lester it was decided that sample and hold amplifiers (S/H) should be used. The basic ingredients of an S/H circuit are op-amps, capacitors and a FET switch. Basically a voltage is fed into the S/H during the sample stage, and a capacitor is charged. Then when the hold stage is executed i.e. FET switch

disconnected, the capacitor holds the voltage that it got to. The trade off in S/H circuits is between the acquisition times, the time in which it takes to charge the capacitor, and the “droop” rates, the rate at which the capacitor loses voltage. A diagram of sample and hold steps and the concept of acquisition time and droop rate is shown in Figure 7.4.1.

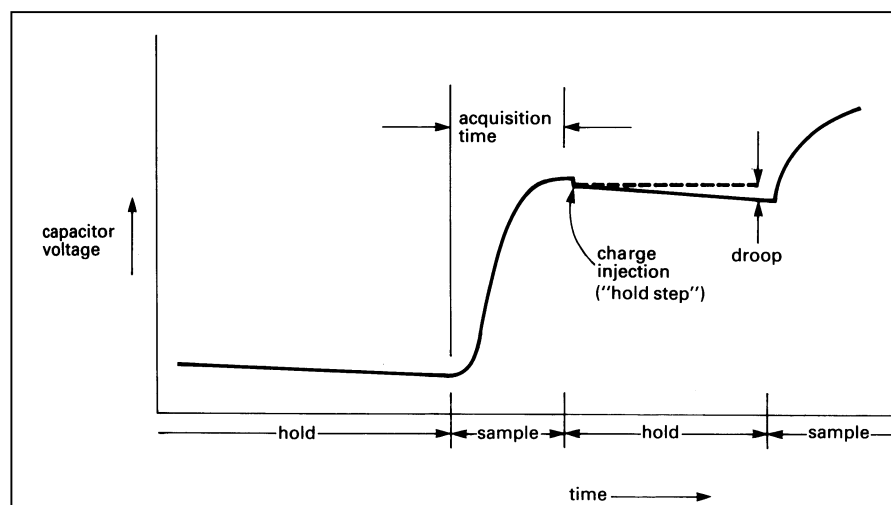


Figure 7.4.1. Sample and Hold Relationships [45]

When selecting an S/H the determining factors were, low acquisition time, $\pm 10V$ voltage range, and price. Based on these factors the HA-5320 manufactured by Harris Semiconductor was chosen. They were purchased in a quantity of 10 to get a discounted price of £4.64 each instead of £5.80 [43] and allow for spares. For more information on the HA-5320 see [Appendix 11].

7.5 Decoder Interface

As discussed in Section 6.1 the IMU outputs information in RS-422 format. Therefore to get a clean signal into the IMU decoder a RS-422 decoder was required to take the dual output from the IMU and output a single line which displays accurate TTL logic level. The chip chosen for this application was an MC3486 quadruple differential line receiver with 3 state outputs, manufactured by Texas Instruments at a cost of £1.08 [43]. The determining factors were that it can take 3 sets of inputs and it was inexpensive. For more information on the MC3486 see [Appendix 12].

7.6 Decoder Component Relationship and Timing

After all the main parts of the IMU decoder were selected the next stage was to work out how each chip would interact with the others. This involved understanding the requirements for each pin on every chip. Also the timing of the whole circuit was crucial as the data has to be decoded concurrently and placed into the correct chips at the correct time. All the timing had to work from the sync and clock signals of the IMU.

One example to illustrate this is the S/H control pin. As each S/H is set to hold the voltage from a particular sensor this pin must be controlled in some way by the 4-16 decoder. This pin effectively tells the S/H to ‘sample’ when a logic level of zero is

present and to 'hold' when the logic level is one. Therefore the S/H control line must be taken low after the data has been converted by the DAC and the DAC output is present on the S/H input. It also must remain low for the duration of the acquisition time of the S/H, which is dependent on the external hold capacitors. The control pin must also bare some relationship to the sync line as the sync indicates when all the information from a sensor has been sent.

The way in which this was achieved can be seen in Figure 7.6.1. It required the use of a monostable, a NAND gate and a NOT gate. The NOT gate inverts the sync for the write pin on the DAC as it is active low, this makes sure that all the information on the DAC gets converted and is made available on the S/H input. The sync also goes to a monostable which outputs an increased pulse length of the sync. The length of this pulse is set by the RC constant which has to be greater than the S/H acquisition time. This new sync is then input into a dual NAND gate with the 4-16, so that when the new sync pulse is high and the output from the 4-16 Decoder is high, the S/H will sample. Then when the new sync pulse stops the S/H will hold its voltage until it needs to sample again.

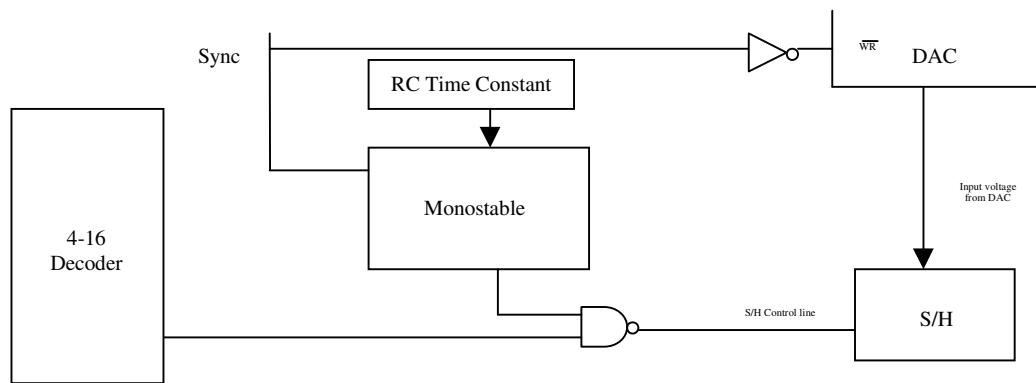


Figure 7.6.1. S/H control Pin Example

The details of the exact relationships between all the chips and the necessary steps taken to ensure that all the timing is correct can be seen in [41]. More information on the Monostable and NAND Gates can be found in [Appendix 13] and [Appendix 14] respectively.

8 IMU Decoder Construction

After all the chips and components had been decided upon and their relationships were determined, the physical construction was done. This involved drafting all the connections between the chips and the power supplies. To do this a detailed analysis of all the data sheets was performed. The datasheets used can be seen in [Appendices 8-14]. Initial construction to see if the design would work was done using matrix board and wire wrapping techniques. Then final construction was performed on Veroboard using soldering techniques. Both versions of the decoder used Wire Wrap (WW) sockets and IC sockets so that the risk of damaging the chips was decreased.

8.1 IMU Decoder Wire Wrap Version

The WW technique was used as the test version as it was believed to be quick and easy, as it would eliminate the problems of dry solder joints and track cutting which are associated with other methods. Construction started by getting a single piece of matrix board and then placing all the necessary WW sockets on it, in a logical order as to minimise the length of wire required. Then unwanted areas of the matrix board were broken off, this reduced the size of the board which would be more suitable for platform use.

Once all the chips and components were placed, a diagram of all the chips and their pin descriptions was made, but in the reverse of the front view, as all the wiring would have to be done on the back of the board [Appendix 15, Figure 15.1]. From this diagram the chips were connected up using a colour coding system which would allow for easy tracking of wires. The colour coding system used was:

- Black = Ground
- Red = 5V
- Pink = 15V
- Blue = -15V
- Purple = Data before DAC
- Green = Sync
- White = Clock
- Yellow = Data after DAC

Initial construction was slow as a result of having to count the pins on each chip before a wire was wrapped; this was done to make sure that the wire was correctly placed. The pace of construction increased as more wires were added as there were less pins to get mistaken with and the speed of attachment increased with practice. The early stages of construction can be seen in Figure 8.1.1a and the later stages of construction can be seen in Figure 8.1.1b.

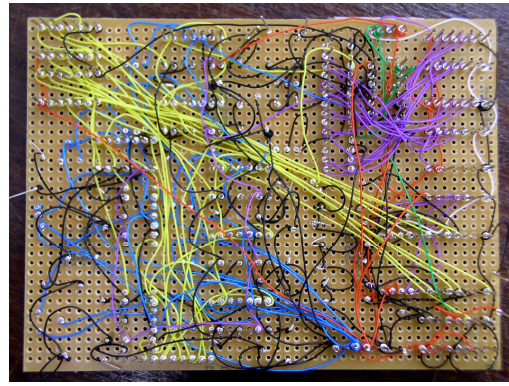
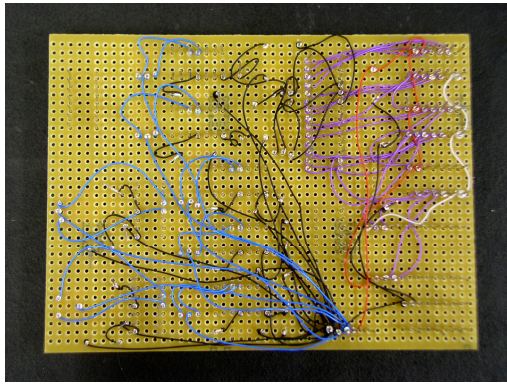


Figure 8.1.1a. Early Stages in Construction Figure 8.1.1b. Later Stages in Construction

As can be seen from Figure 8.1.1a and 8.1.1b, the back of the board becomes very untidy. This makes the tracking of wires very difficult as there can be up to 10 wires overlapping in certain areas.

During construction alterations had to be made due to initial mistakes at the design process, therefore the layout had to be changed. This involved unwrapping, moving, and rewrapping many of the current components to accommodate for new ones. It would have been easier to implement these changes if the board hadn't been reduced in size. Moving these components was a timely task and involved more work than initially anticipated. As each wire was cut to approximately the exact size required. Moving the component normally required adding a completely new wire as the old one was often found to be too short. If the wire was still the right length it would sometimes brake upon rewrapping as the wire suffers from fatigue. Most pins also had more than one wire on them, so to remove one wire it often required the unwrapping of many more or the cutting of the existing wire which once again could make it too short.

The final front view of the decoder can be seen in Figure 8.1.2. This clearly shows the limited space that was worked in. There are 4 inputs going into the board which were designed to power the board i.e. $\pm 15V$, Ground, 5V. There were another 3 inputs which come from the IMU i.e. Clock, Sync, and Data. Finally there were 8 outputs coming from the board one from each S/H.

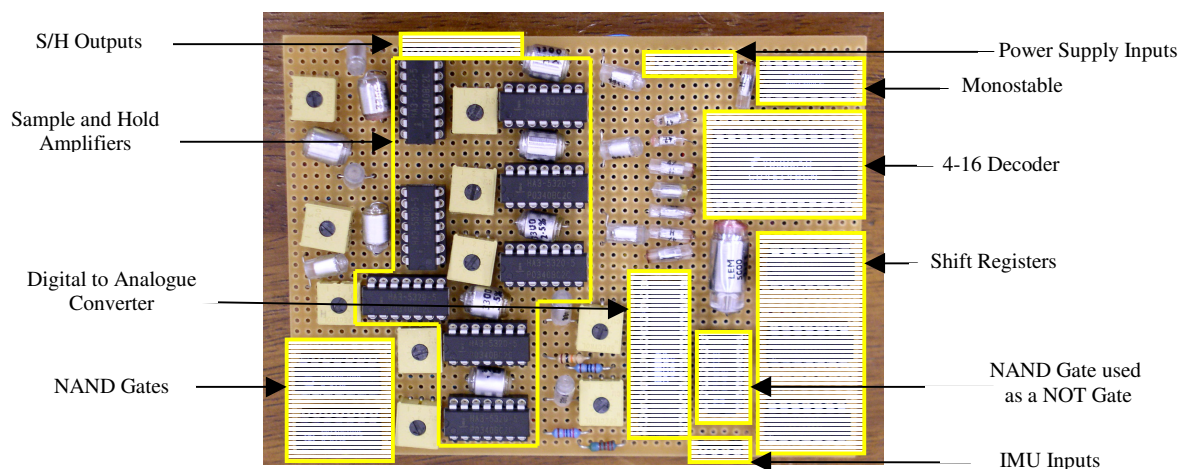


Figure 8.1.2. WW Final Construction

The outputs pins were connected in a logical sequence in order to establish which pin was which sensor. This sequence can be seen in Figure 8.1.3.

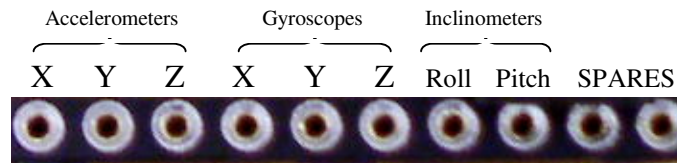


Figure 8.1.3. Logical Output Sequence

8.1.1 WW Decoder Testing and Debugging

There were several different methods used for testing. The first was a continuity check across the pins, without the chips in their sockets. This was done to make sure that the majority of pins were connected up correctly and that there were no short circuits. It also pointed out any bad connections. After this was done and everything appeared to be in order, the shift registers were inserted into their correct positions. Then a simple push button testing board was constructed [41]. The board consisted of two push buttons, one for clock and one for sync, a dil switch to set the input bit, and a monostable to stop the switches bouncing. This was used in conjunction with an oscilloscope to check all the outputs from the shift registers when a set signal was inserted, see Figure 8.1.1.1. Information on the values inserted by the push button method and the expected results can be found in [41]. After the shift registers were checked and were working, the 4-16 Decoder was inserted and this was also checked and found to be working. Then finally the DAC and the S/H were inserted and tested, initially these did not give out the expected outputs. This resulted in analysing the data sheets and circuit diagram further. As a result several wiring and design faults were found. These were rectified and testing was carried out again, but still several aspects of the decoder were not working correctly.

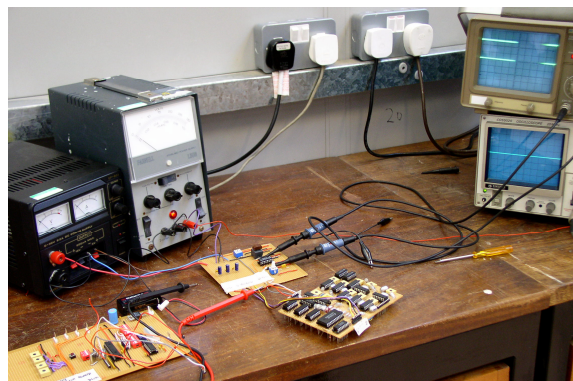


Figure 8.1.1.1. WW Test Setup

It was not understood why some of the S/Hs were not working correctly, first impressions were that it was a timing fault. As the test board was very restricted in its functions another method of testing was required. This brought about the IMU emulator. The IMU emulator is PIC which has been programmed to simulate the timing of the IMU whilst outputting a set range of voltages on each S/H, its design and construction can be found in [25], the emulator is also discussed further in Section 8.2.1.

As A.Tombling designed and constructed the emulator, he was present at its first testing with the WW decoder. Initially when the emulator was first connected the decoder did

not output for expected results. This gave the indication that there were still some inaccuracies in the circuit design. Therefore a further collaborated analysis of the circuit design and datasheets was performed, this once again proved to be useful as several more wiring and design faults were found, which had been overlooked before.

Finally all the corrections were made and testing was carried out by both the basic push button method and emulator and the decoder was found to work.

8.2 IMU Decoder Veroboard Version

Once all the initial errors had been discovered using the WW version it was decided that a Veroboard version should be made, as it would be more suitable for platform use. It would be more suitable for platform use because the connections on the WW version were likely to come loose when subject to the vibrations from the IC engines.

Once again before construction started, IC sockets were placed on the Veroboard to establish chip position. It took a considerable amount of time to position the sockets, it was done in such a way that the copper tracks on the Veroboard were used to the maximum efficiency, which in turn reduces the number of external wires that are needed and the amount of tracks that had to be cut. This time sufficient space was made available so that if the board needed adding to it would not be too difficult to do so. After the chip placement was decided upon a detailed circuit diagram was hand drawn with the chips positioned exactly the same as they are positioned on the board [Appendix 15, Figure 15.2].

Construction was a timely process and it involved a lot of care and concentration. Attention was paid to all solder joints to make sure they were not ‘dry’ and care was also taken not to accidentally solder tracks together. Masking tape was added to the board in order to label the chips and the various power supply lines. A great deal of effort was also put into keeping the board as neat and tidy as possible so that if debugging were necessary it should be relatively easy to do. The completed Circuit can be seen in Figure 8.2.1. The completed version with the components labelled can be seen in [Appendix 15, Figure 15.3].

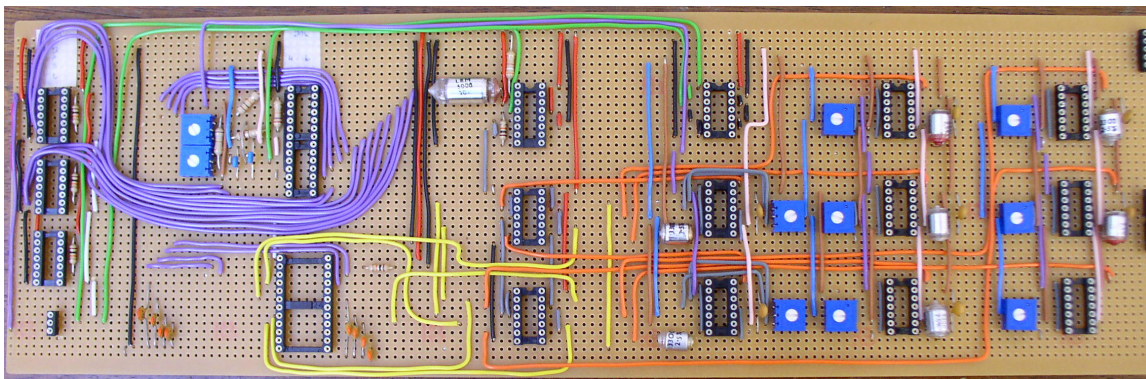


Figure 8.2.1. Veroboard Final Construction

The wires were colour coded as follows:

- Red = 5V
- Black = 0V (of the 5V supply)
- Pink = 15V

- Brown = 0V (of the 15V supply)
- Blue = -15V
- Yellow = Data from the 4-16 Decoder & NAND gates
- Orange = Data from the S/H to the outputs
- Grey = Feed back loop within the circuit (S/H mainly)
- Purple = Data from the IMU and the Shift registers
- Green = Sync from the IMU
- White = Clock from the IMU

Note that the two 0V grounds were connected together and several decoupling capacitors were added to the supply rails, after conversations with Dr G.A. Lester and J. Andrews and further research [46], the decoupling capacitors chosen were, 10 μ f electrolytic and 100nf ceramic.

After all the wires were attached, the tracks of the Veroboard were broken, so that all the tracks used were as short as possible. This was done to make sure that there were no accidental short circuits, and it also reduced the level of unwanted noise.

8.2.1 Veroboard Decoder Testing and Debugging

Once again a continuity test was performed first. As a result a very small amount of wiring errors were highlighted, which were consequently fixed. Then the next stage of testing was to use the push button test board, more details on the procedure taken can be seen in [41]. This found a few more minor errors, but this was expected due to the number of wire connections present, and again these were consequently fixed. The debugging of this board was a lot simpler, as all of the design faults had been discovered in the previous WW version. Also it was a lot easier to follow the tracks and wires due to the better layout, although this layout did utilise a lot of space.

After the Veroboard decoder was tested with the push button test board and was working as expected, the IMU emulator was attached and all the outputs were viewed on an oscilloscope. See Figure 8.2.1.1a and 8.2.1.1b.

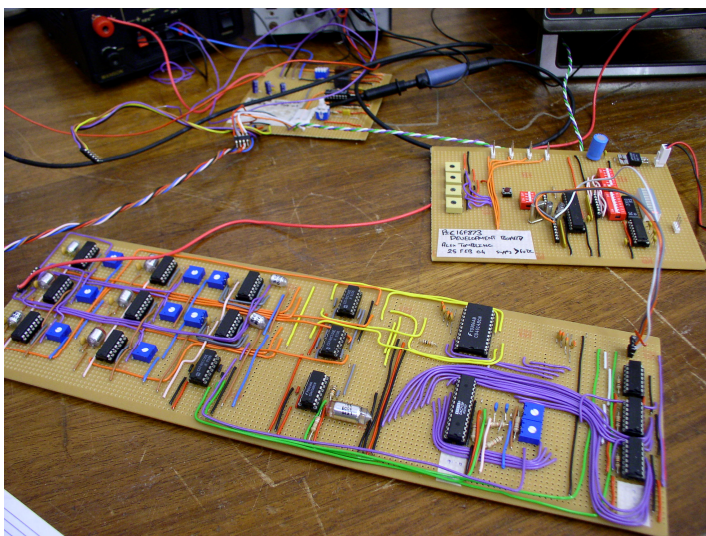


Figure 8.2.1.1a. Emulator Test Setup

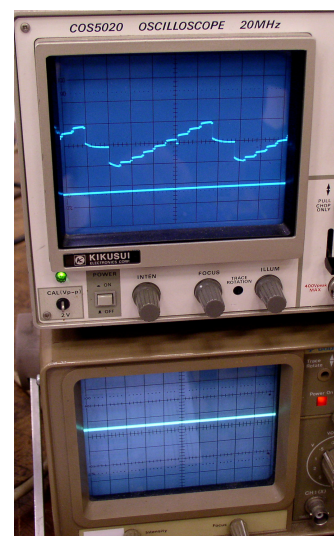


Figure 8.2.1.1b. Oscilloscope Outputs

The top oscilloscope in Figure 8.2.1.1b shows the data coming out of the emulator and the bottom oscilloscope shows the level of one of the output pins. Each pin was tested and compared to the expected output. The output pins should all remain at a constant voltage for the emulator was designed to repeat a signal, which set each of the output pins to different levels. These levels can be seen in Table 8.2.1.1.

Output Pin	Sensor	Voltage (V)
1	X, Accelerometer	2.5
2	Y, Accelerometer	5
3	Z, Accelerometer	7.5
4	X, Gyro	-5
5	Y, Gyro	-7.5
6	Z, Gyro	-2.5
7	Roll Inclinometer	10
8	Pitch Inclinometer	-10

Table 8.2.1.1. Emulator Voltage Assignment

After a few minor alterations to the circuit and the calibration of the potentiometers was done [41] all the outputs from the emulator corresponded to the expected values.

The results of this initial testing meant that the decoder circuit was now fully functional to our knowledge. Therefore the prerequisite of the IMU testing had been complete.

Before the IMU could be tested the RS-422 interface had to be made as well as a 20 pin connector to connect onto the IMU, details of this construction can be found in [41], Figure 8.1.2.2 shows the RS-422 construction and Figure 8.1.2.3 shows the 20 pin connector.

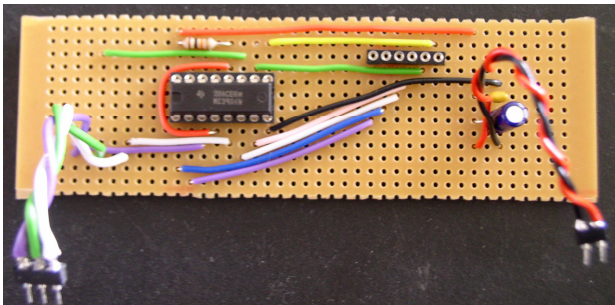


Figure 8.2.1.2. RS-422 Interface

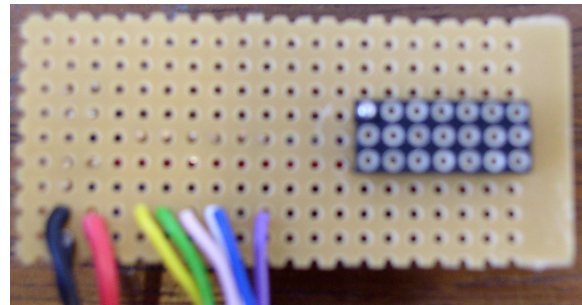


Figure 8.2.1.3. 20 Pin Connector

Once the interface was complete the IMU was attached and the outputs were viewed. The results that were obtained were not expected see Figure 8.2.1.4. Instead of the outputs being at constant 0V for the accelerometers and gyros, whilst the IMU is stationary, it was all very unstable. The same applied to the inclinometers, there was no obvious correlation between the movements of the IMU and the output from the decoder. The first action taken was to try and reduce any noise levels present on the board by adding more decoupling capacitors and making the tracks as short as possible.

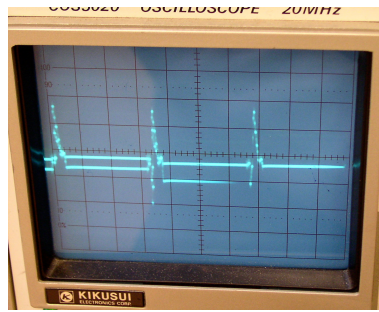


Figure 8.2.1.4. Decoder with SilMU0X Output

The noise levels were reduced but it still did not solve the problem. The next stage which was successful was to use a Data Analyzer. A Sony Tektronix 308 Data Analyzer was used to determine what was in the header field i.e. what identity words was the IMU inputting into the decoder. The trigger of the analyzer was attached to the sync line to make sure that all the data had been clock through before sampling occurred. Four sample lines were attached to the input on the 4-16 Decoder and the ground was attached to the ground on the board, see Figure 8.2.1.5. When the analyzer sampled the results viewed were not expected, see Figure 8.2.1.6. The most significant bit of the identity word was never high; this implied that either the data analyzer was not working correctly or that the information never got into the last bit of the shift register.

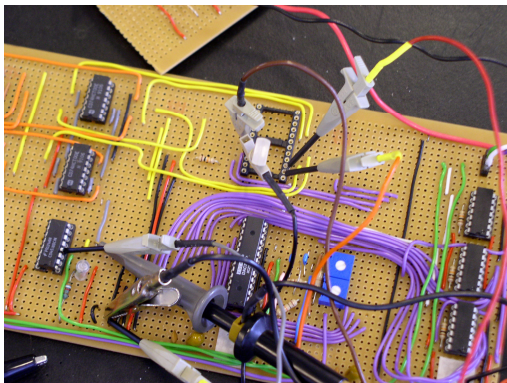


Figure 8.2.1.5. Data Analyzer Connection

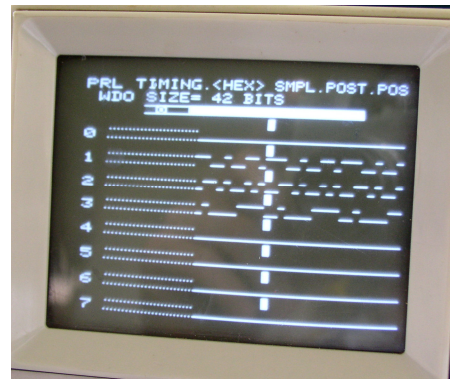


Figure 8.2.1.6. Initial Analyzer Output

To see if the analyzer was working correctly the IMU emulator was attached, this proved conclusively that the data analyzer was working correctly and that there should be high pulses in the most significant bit.

The next plan of action was to connect the IMU back up and record all the values in the identity segment of the header field when the sync was triggered, this was done in Hex. Then a table was constructed which consisted of 24 rows, one for each of the data bits, and 15 columns, 11 for each of the serial words plus 3 to see if the pattern repeats.

The trigger of the data analyser was then attached to the clock, which would show value of the identifier after every clock pulse. The data analyser was turned on and data was then input into the table constructed so that the rows in the table would represent the sequence of transmission. From this table it could be seen that the sequence that was obtained when the sync was triggered was on row 24, which would be correct, but it also

showed that the sequence that was expected was on row 1 which indicated that data was 1 clock cycle behind.

After further investigation of the timing diagram, it was realised that the data was clocked in on the negative clock edge. The IMU emulator worked because it was built to our initial interpretation of the IMU operation. To rectify the problem the clock was inverted before it went into the shift registers, and the strobe on the 4-16 Decoder was triggered off the sync instead of the clock. After these alterations, it could be seen that the decoder worked with the IMU and the output pins were giving the results expected. The final circuit diagram can be found in [Appendix 15 Figure 15.4]

9 IMU Testing

After it was established that the IMU decoder circuit worked, more meaningful results were required to see how well the IMU would work within the control system. This involved many aspects, the first was to build a test rig that would enable accurate measurements to be taken, the second was to design and build integrator circuits that would be able to convert the acceleration from the accelerometers into displacement for the height measurements and the rotational velocity from the gyros into angles for tilt measurements. This report mainly focuses on the design and construction of the test rig and covers some aspects of the testing, the design and construction of the integrator circuits can be found in [41].

9.1 IMU Test Rig

To test the IMU accurately a rig was needed. The requirements of the rig were that it had to hold the IMU in the correct orientation and maintain it with no intervention. It had to be able to rotate the IMU in the Pitch and Roll axes, with the rotation point being at the centre of gravity (CG) of the IMU. It had to have a measuring device in order to obtain the angle of rotation of up to $\pm 90^\circ$, and it also had to accommodate for the connector and wires.

There were several initial designs, but due to time constraints the simplest design was chosen. It consisted of base unit, a 2-Axis rotational centre piece, and a clamping mechanism, the CAD designs can be seen in [Appendix 16]. The base unit comprised of three parts, a bottom section for stability and two side sections at right angles to the base to hold the centre piece. The side sections had a semi-circular groove at the top with a radius of 3mm, which allowed a rod of 6mm diameter to be placed and held.

The centre piece comprised of three parts, a large section which would accommodate the IMU, it contained four holes, a large centre hole for the IMU to protrude through, and three smaller holes to allow the IMU to be bolted on. The large section also had a circular section of a set depth cut out in which the IMU would sit in order to get the CG in the very centre of the section. It also contained two 6mm rods placed at either side to allow for Pitch rotation. The two smaller sections of the centre piece were attached onto the large section at right angles and each had a 6mm rod protruding from them, this enabled Roll rotation.

The clamping mechanism enabled the centre piece to be rotated with an initial force, and then stay at that position. It consisted of two sections which screw onto the base unit, each section also has a 3mm radius groove enables the 6mm rod to be placed between it and the base unit. The ease of rotation is dependant on how tight these sections are tightened.

Before the structure was constructed, the dimensions of the IMU were obtained both by physical measurement and by the drawing provided by BAE Systems. These measurements were then used to create an AutoCAD drawing [Appendix 16]. Figure 10.1.1 shows a rendered version of the drawing which will enable rotation in the Roll Axis. After the drawing was complete construction started, the material used was wood as it is relatively easy to work with and the structure would not be subject to large forces. A ban saw was used to cut out the sections, a pillar drill was used to drill all the holes

and grooves, and a lathe was used to extract out the circular section of a set depth in the large centre section. The components of the rig can be seen in Figure 9.1.2.

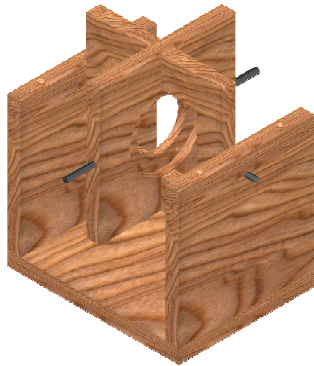


Figure 9.1.1 Rendered CAD Drawing

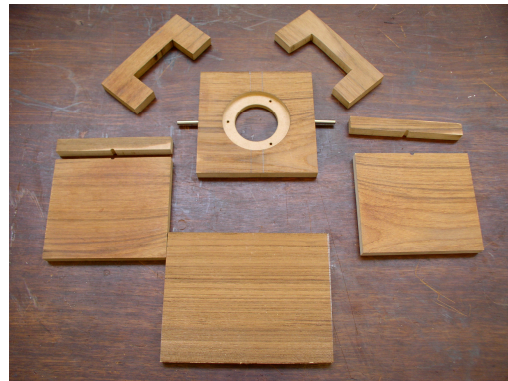


Figure 9.1.2 Components before Assembly

The components were attached together using right angled brackets and 4mm wood screws, and 5mm wood screws were used to clamp the centre piece down. The last component to add to the structure was a protractor, in which a 6mm hole was drilled through its centre. It was attached to the left hand side section of the base unit using UHU glue, its centre was positioned so that it was directly in line with the CG of the IMU. Lines were then drawn on the edges of centre sections which indicated the planes about the CG. This was found to provide an adequate level of accuracy, see Figure 9.1.3. The completed structure can be seen in Figure 9.1.4.

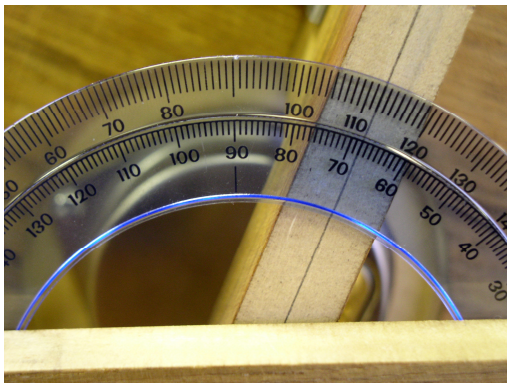


Figure 9.1.3 Accuracy of Measurement



Figure 9.1.4 Final Construction

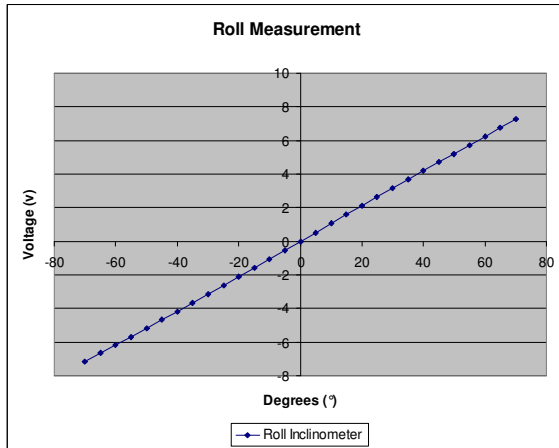
The test rig was found to be more than suitable to be used for the testing the IMU. Its main limiting factor was that it could not easily test the Z-gyros i.e. Yaw, but this could be overcome.

9.2 Testing and Conclusions

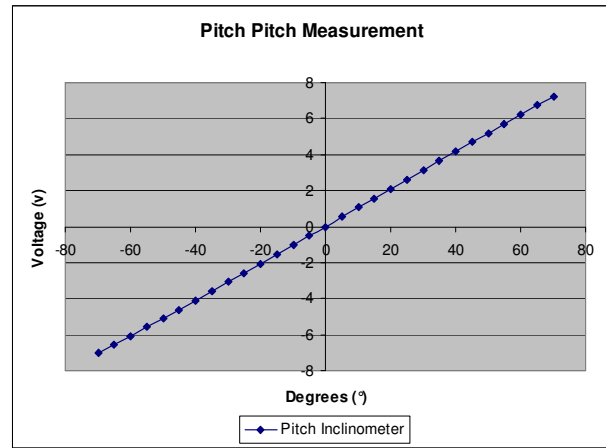
There were a total of eight sensors that needed testing. This report concentrates on the inclinometers to see if the decoder circuit and test rig were successful in performing their functions. Further testing of all the outputs, and detailed analysis of all the test results can be found in [41].

To test the inclinometers the IMU was placed in the test rig and then attached to the decoder circuit. The Roll inclinometer was tested first; to do this a multi-meter was attached to the Roll inclinometer output pin which enabled a voltage to be read. The

IMU was then rotated until the multi-meter read 0V; this then formed the centre from which to rotate the IMU. This centre was at 87° according to the protractor. The IMU was then rotated to $\pm 70^\circ$ at 1° increments and measurements were recorded. The results of this test can be seen in Graph 9.2.1. This process was then repeated for the Pitch inclinometer where the centre is at 91° . The results of this test can be seen in Graph 9.2.2.



Graph 9.2.1 Roll Inclinometer Results



Graph 9.2.2 Pitch Inclinometer Results

This testing proved that the decoder circuit worked as it constantly output a set voltage corresponding to the angle of inclination. It also confirmed that the test rig design was successful as the orientation of the IMU could be changed by 1° increments with ease and the IMU held its position with no intervention. Pictures of the Pitch inclinometer testing can be seen in Figures 9.2.1 and 9.2.2.



Figure 9.2.1 Pitch Inclinometer (+°)



Figure 9.2.2 Pitch Inclinometer (-°)

During the testing of the accelerometers and gyros it was discovered that the majority of the sensors have been internally compensated [41]. Therefore the expected results were not obtained. T. Moy from BAE systems was unfortunately unable to provide more information on the algorithms that have been implemented, which in turn has reduced the range of outputs that can be used or manipulated. For more information on this see [41]. The recommendations for next year would be to either use another IMU in which there is no internal compensation, or to use one which has internal compensation and the documentation to back it up. Failing that I would advise next years group to use a single sensor arrangement as was done in the previous year, but to use the latest gyros and accelerometers as technological advances have improved the quality of these components significantly over the last year.

10 Overall Conclusion

In Conclusion, the design and development of a flying platform was an extremely challenging, yet enjoyable and enormously rewarding project. Although the platform never became airborne, a lot of the initial tasks set were completed.

The management of the project was implemented well, and the communication networks were setup effectively. This in turn enabled the project's progress to be viewed from anywhere at anytime, providing a computer and an internet connection were present.

The propulsion goals were met with a degree of success, for an IC engine was purchased and fully tested. Testing proved that the current methods would not be suitable for flying the platform and a payload, and suggestions for further investigation were made.

The design and construction of the IMU decoder circuit was a success, for it met its specification, which was to decode the IMU's outputs correctly. The reason why it could not be implemented into the control system was because of the internal compensation algorithms implemented by BAE systems. Suggestions were made for future directions and a good insight into the problems of design and construction were conveyed.

Appendix 1

Initial PDS

	This design
Performance	<ol style="list-style-type: none"> 1. Must hover approximately 1 m above the ground. 2. Flight duration to be approximately 20 minutes. 3. Must remain Stable. 4. Must provide viable operating platform. 5. Must be able to carry a payload of up to 3 kg. 6. Must have the capability to have the On/Off controlled by remote.
Environment	<ol style="list-style-type: none"> 1. Must be capable of operating in a temperature range of -10°C to 50°C. 2. Must be capable of operating in humid conditions and to be water resistant when operating in light rain. 3. Must be operated in minimal air flow disturbances i.e. minimal wind speeds.
Maintenance	<ol style="list-style-type: none"> 1. Onboard battery must be easily attainable for possible replacement, and recharging. 2. Fuel tank for internal combustion engine must also be easily accessible for refueling.
Life in Service	<ol style="list-style-type: none"> 1. Products life in service is to be approximately 5 years.
Target Production Cost	<ol style="list-style-type: none"> 1. A budget of £1000 has been assigned to this project.
Size	<ol style="list-style-type: none"> 1. The flying platforms dimensions to be similar to the dimensions specified in the previous groups report.
Weight	<ol style="list-style-type: none"> 1. Yet to be determined but should be designed for minimum weight possible. Estimated weight including payload is approx 10 kg.
Materials	<ol style="list-style-type: none"> 1. Materials used must have a high mechanical tolerance, and must have as lower density as possible.

	This design
Design Constraints	<ol style="list-style-type: none">1. The flight must be completely autonomous.2. The design must not a helicopter based design.3. Must use an onboard IC engine for power generation.

Appendix 2

Meeting Agenda



University of Exeter
School of Engineering
Agenda
for the
Flying Platform Project Meeting 34
to be held on
Thursday 04 March 2004
commencing at **10.00** am, room 102A

Circulated to: Liam Dushynsky (LD), Richard Forder (RF), Richard Holbrook (RH), Rebecca Hughes (RCH), Kevin Lewis (KL), James Mackenzie-Burrows (JMB), Jody Muelaner (JM), Chris Pozcka (CP), Alex Tombling (AT), Dr. Martin Jenkins (MAJ), Dr. Gary Lester (GAL).

- 04/03 34.1 Apologies for absence
- 04/03 34.2 i Minutes of previous meeting
 ii Matters arising
- 04/03 34.3 Chairman's Report
- 04/03 34.4 Secretary's Report
- 04/03 34.5 Treasurer's Report
- 04/03 34.6 i Control / IMU
 ii Propulsion
 iii Electrical Power Systems
 iv Platform Structure
- 04/03 34.7 Any Other Business
- 04/03 34.8 Date, Time and Place of next meeting

Time Meeting Started _____ Time Meeting Finished _____

Appendix 3

Example of a Meetings Minutes



Fourth Year Group Project

Minutes

Date: 04/03/2004
Room: 102A
Meeting: 34

Group Members		Present	Apologies
Liam Dushynsky	LD	✓	
Richard Forder	RF	✓	
Richard Holbrook	RH	✓	
Rebecca Hughes	RCH	✓	(arrived: 10:10)
Kevin Lewis	KL	✓	
James Mackenzie-Burrows	JMB	✓	
Jody Muelaner	JM		✓
Chris Poczka	CP	✓	(arrived: 10:12)
Alex Tombling	AT	✓	
Guests			
Dr. Martin Jenkins	MAJ	✓	
Dr. Garry Lester	GAL	✓	

The Chair welcomed the group to the Flying Platform meeting.

4/3 34.1 Apologies:

4/3 34.1.1 No apologies were received from JM.

4/3 34.2 Previous Minutes:

- 4/3 34.2.1 The minutes from Meeting 32 were accepted by everyone present.
- 4/3 34.2.2 MAJ asked if OS have been emailed. RH said that he sent an email last week and they replied recommending just tightening the screws. MAJ thinks that because the cylinder head is not directly in the airflow, it is getting too hot. This could also be having an effect on the life span of the glow plugs. RH suggested cutting away a section of the duct to increase airflow. MAJ agreed with this.
- 4/3 34.2.3 RCH has spoken to Mike Belmont about the simulation of the platform. He recommended modelling the platform with 3 dimensional vectors. However, this will take too much time to complete. GAL advised that this could be work for next year and just to concentrate on the current mathematical model. KL agreed and said that he quickly needs some information from this for the control section. KL will liaise with RCH today about his requirements.
- 4/3 34.2.4 For the benefit of the guests, LD mentioned that the IMU circuit has been debugged with help from AT. RF explained that all sample and hold units get hot when the sync pulse goes high. This would imply that there is a problem with the inputs as these are common to all units.
- 4/3 34.2.5 No one has seen JM since Monday and therefore no one knows if the central fan will cost anything.
- 4/3 34.2.6 AT has not been able to complete the remote control unit as debugging the IMU circuit was the priority.
- 4/3 34.2.7 RH informed the group that the coupling for the genset was now complete. Once the electronics section is finished then genset testing may begin.
- 4/3 34.2.8 The IMU testing has not been completed due to the issues with the IMU circuit. It is hoped that the IMU can be fully tested by the end of next week.

- 4/3 34.2.9 RCH has modelled the flow through the central fan duct as a result of CP's structural design and a handout was distributed at the meeting.
- 4/3 34.2.10 KL has not been able to complete the report into temperature compensation as he has been concentrating on integrator design and implementation.
- 4/3 34.2.11 LD has nearly completed the Vero board circuit and aims to have this completed by today.
- 4/3 34.2.12 RH has bought an improved mix of fuel for the IC engines.

4/3 34.3 Chairman's Report:

- 4/3 34.3.1 LD requested that everyone looks at the CPA on the workshop
- 4/3 34.3.2 In the project review, LD is confident that the project will come together within the time available. However, MAJ warned that there is no structural drawings or design and this is the weak link.
- 4/3 34.3.3 As it looks likely that group members may need to access the building out of hours, LD requested that everyone gets an out of hours form today.

4/3 34.4 Secretary's Report:

- 4/3 34.4.1 The secretary had no matters which needed discussing at the meeting.

4/3 34.5 Treasurer's Report:

- 4/3 34.5.1 As KL is about to produce another balance sheet, he requested that everyone sends any outstanding lists of components to him.

4/3 34.6 Matters Discussed:

i) Control / IMU:

- 4/3 34.6.1 MAJ asked if there was a test procedure for the IMU. LD said that a partial one had been completed but further work still needs to be done.
- 4/3 34.6.2 KL reminded RF that the cosine rule needed revising as this is required for compensation between axes.
- 4/3 34.6.3 KL enquired as to progress of height control. LD asked RCH but she had no knowledge that this task was assigned to her. She was reminded that this can be seen in the minutes from meeting 27 under section 27.6.5. GAL said that using the signal to control height would be straight forward. The problem is getting the signal. RCH agreed to look into this over the next two weeks.
- 4/3 34.6.4 Depending on the success of the Vero board circuit, LD and RF hope to start manipulating signals from the IMU by Monday.

ii) Propulsion:

- 4/3 34.6.5 RH explained that 4kg of thrust was obtained from the central fan. RCH was surprised at this result. However, RH hopes that this could be increased with the improved mix of fuel. There are also some more glow plugs on order from OS.
- 4/3 34.6.6 RCH suggested adding weight to balance out the genset on the platform. RH does not agree with this as it might increase the quantity of fuel required. RH is interested in mounting the genset under the central fan to improve stability. The central fan will also help cool this as well.
- 4/3 34.6.7 MAJ suggested mounting the genset at 90 degrees with a propeller to achieve additional thrust as well as cooling.

iii) Power Systems:

- 4/3 34.6.8 JMB explained that he is revising the original genset circuit as the first one was not sufficient. He hopes to have this complete ready for the next testing session.

CP explained that he is refining the original genset circuit as the first one was not sufficient. He hopes to have this complete ready for the genset testing on Monday.

iv) Structure

- 4/3 34.6.9 CP explained that he would like to know what total thrust the platform can give so as to calculate the minimum weight for the structure. MAJ reminded the group that all weight needs to be kept as low as possible.
- 4/3 34.6.10 KL warned about not wasting time and increasing weight by making an adaptive platform. This would only be needed if JM's fan seemed likely to be used. At this point the chairman put forward the following motion: **"Should the group incorporate JM's fan into this year's design"**. All voted against this.
- 4/3 34.6.11 RH then put forward a second motion: **"Should the design be adaptable for JM's fan next year"**. RH and AT were in favour of this. Everyone else disagreed.
- 4/3 34.6.12 CP will draft a timescale of structural design and produce a mock-up for Monday. RH advised speaking to Colin Camp with regards to the timescale. He will then calculate the distribution of weight on the platform for Tuesday depending on the results from the genset testing.
- 4/3 34.6.13 CP requested being emailed when any fundamental changes occur within the project. LD said that most people are present during core time which is when most information is usually shared. He also pointed out that signing in on the board in the workshop would help know the location of all members.
- 4/3 34.6.14 LD asked if CP could construct a technical drawing of the platform for Monday. CP said that he is unsure of how accurate it will be as he does not yet know all the information necessary. GAL pointed out that structural design will be an iterative process and to get a first design completed.

4/3 34.7 Any Other Business:

- 4/3 34.7.1 RH requested informing LD of when they will be available over the Easter holiday.
- 4/3 34.7.2 AT reminded the group to use the IN / OUT board in the factory effectively. GAL said that the factory staff use a computerised one of these and this proves useful in determining the location of people.
- 4/3 34.7.3 AT informed the group of the need to have clearly labelled circuit diagrams. A list of all the current circuits is on WebCT. He also gave GAL a copy of all current circuit designs.
- 4/3 34.7.4 MAJ said that in order to mark the 8 page report correctly, each member will have an interview with himself, Soon Tiam Koo, and Dave Newman to determine the extent of knowledge obtained by that individual. More information will follow.

4/3 34.8 Task List:

Task	Action	Deadline
Complete out of hours form.	ALL	04/03/2004
Completion of Vero board circuit.	LD	04/03/2004
Liase about simulation and control problems.	KL, RCH	04/03/2004
Completion of CFD work on central fan.	JM	04/03/2004
Modify central fan duct to cool cylinder head of flight IC engine.	RH	05/03/2004
Inform LD of when each member will be available over Easter.	ALL	08/03/2004
First AutoCAD drawing of platform structure.	CP	08/03/2004
Produce timescale of structural design and construction.	CP	08/03/2004
Produce mock-up model of platform.	CP	08/03/2004
Complete circuit for genset testing.	JMB	08/03/2004
Manipulation of signals from IMU.	LD, RF	08/03/2004
Give any outstanding lists of components to KL.	ALL	08/03/2004
Investigate the issue of sample and hold units heating.	AT, LD, RF	08/03/2004
Calculating the distribution of weight on the platform.	CP	09/03/2004
Determine how the genset will be mounted on the platform.	RH	09/03/2004
Produce up-to-date balance sheet.	KL	09/03/2004
Obtain results from IMU.	LD, RF	11/03/2004
Investigated remote control method.	AT	11/03/2004
Simulation of platform.	RCH	11/03/2004
Report into temperature compensation for control system.	KL	11/03/2004
Look into how the height signal will be generated for control.	RCH	18/03/2004
Completion of stress calculations on custom central fan.	JM	18/03/2004

4/3 34.9 Next Meeting:

The next group only meeting will be at **10:00am on Monday 8/3/2004 in Room 102A.**

The next formal meeting with guests will be at **10:00am on Thursday 11/3/2004 in Room 102A.**

Meeting closed at 11:22am.

Appendix 4

WebCT

Screenshots

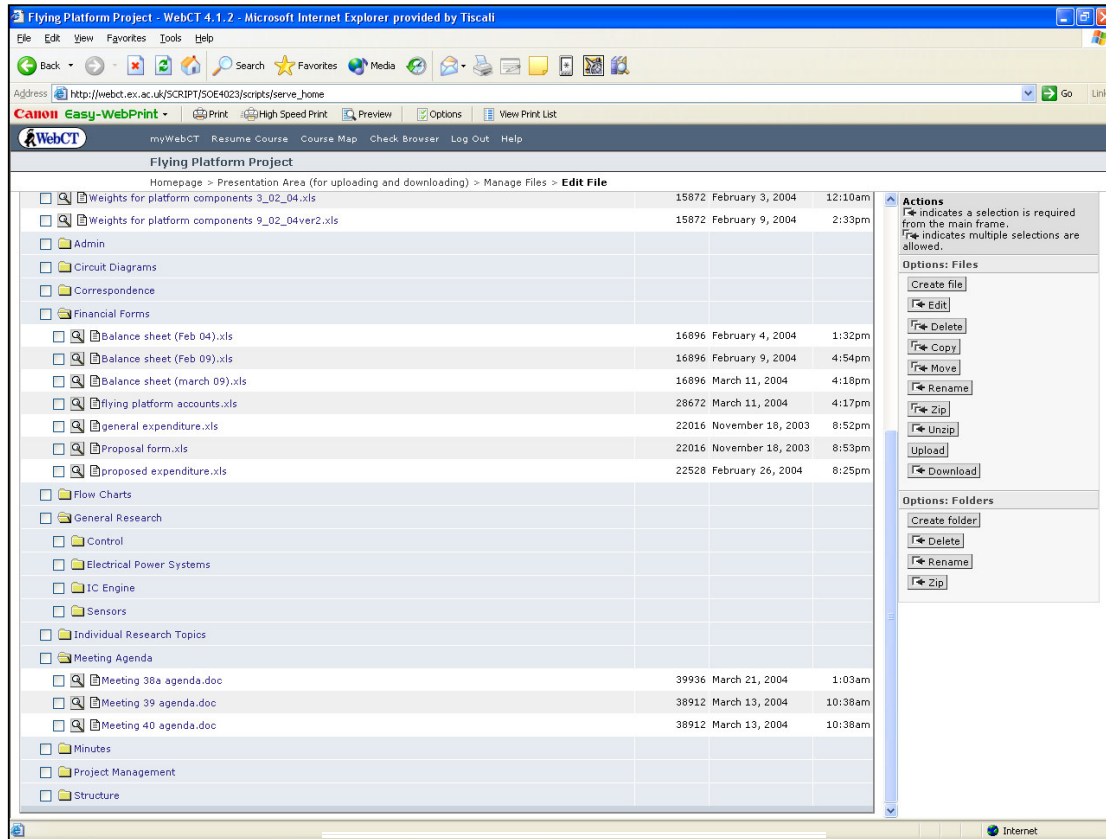


Figure 4.1. Overview of WebCT

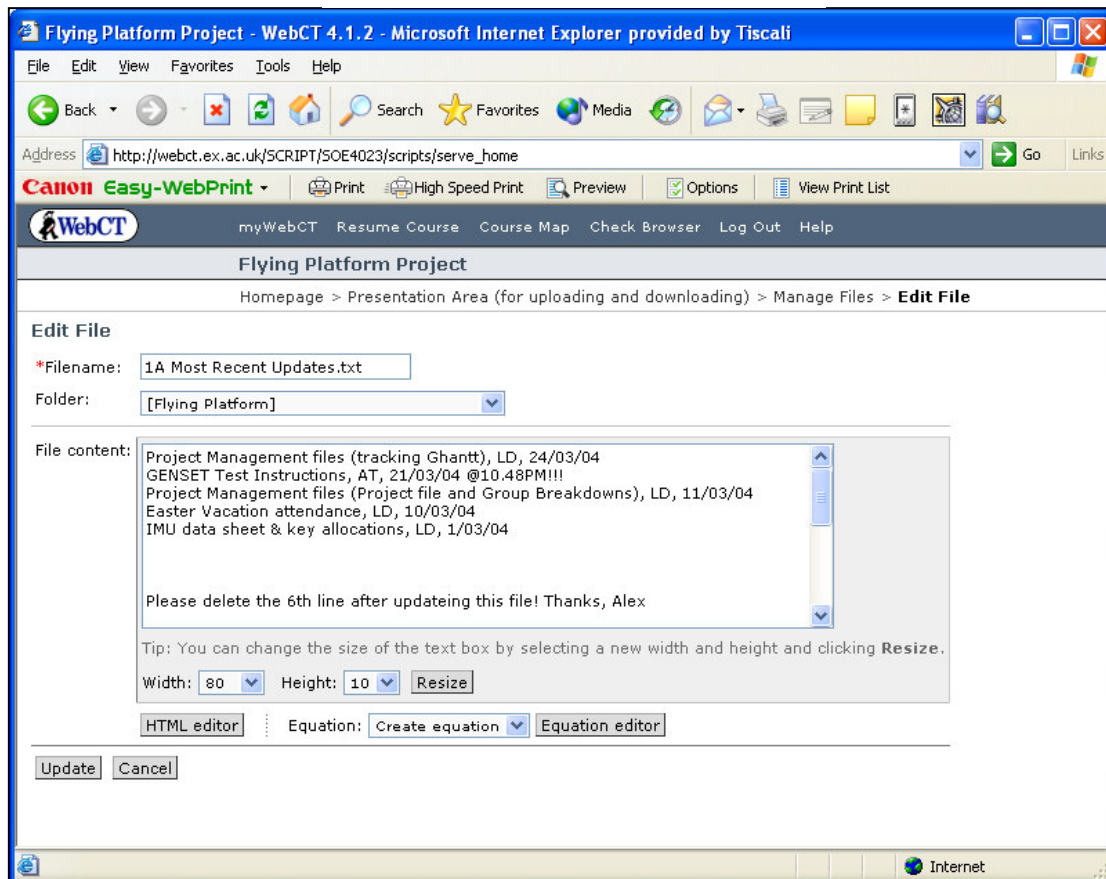


Figure 4.2. Most Recent updates folder

Appendix 5

Project Analysis

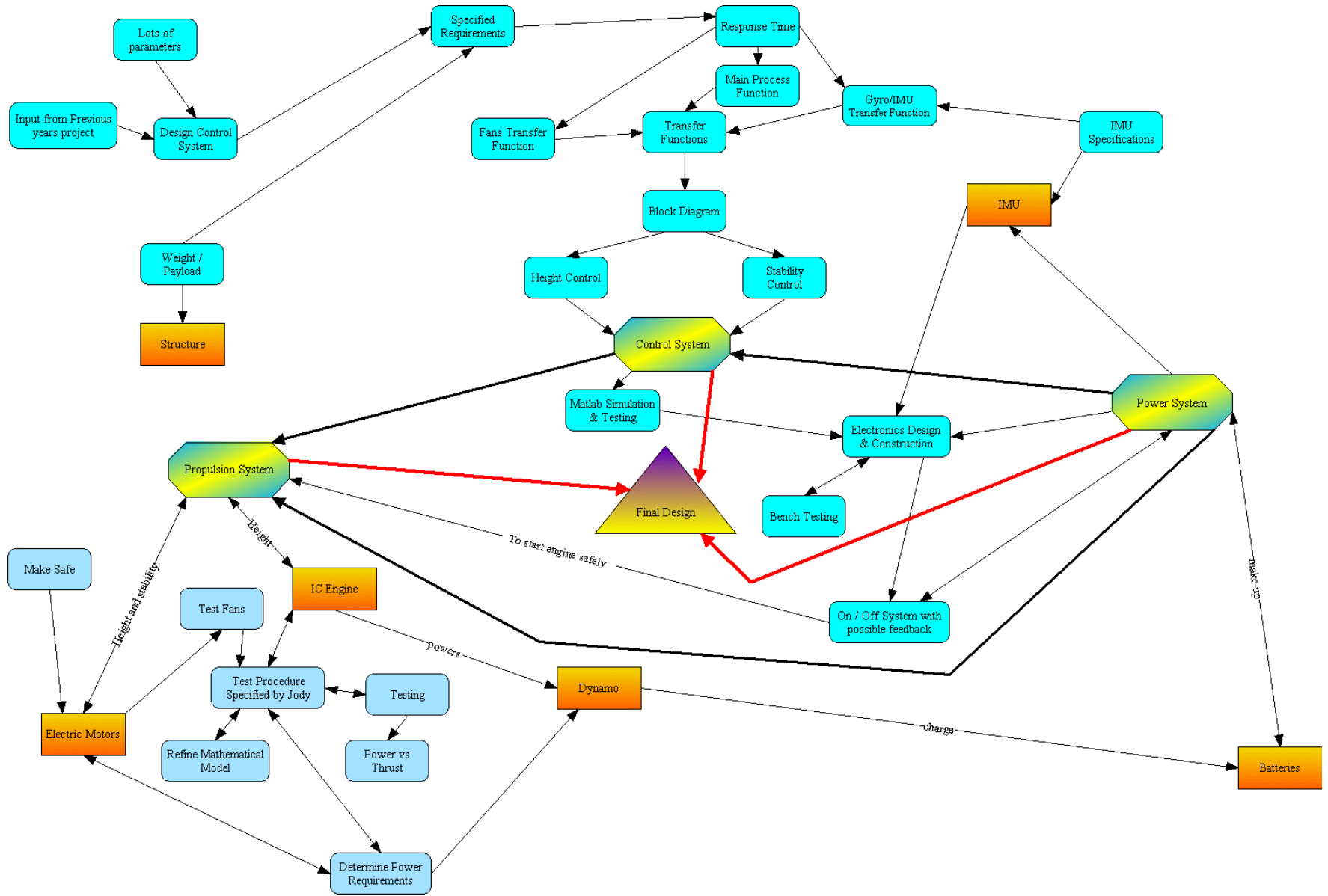


Figure 5.1. Initial Brainstorming

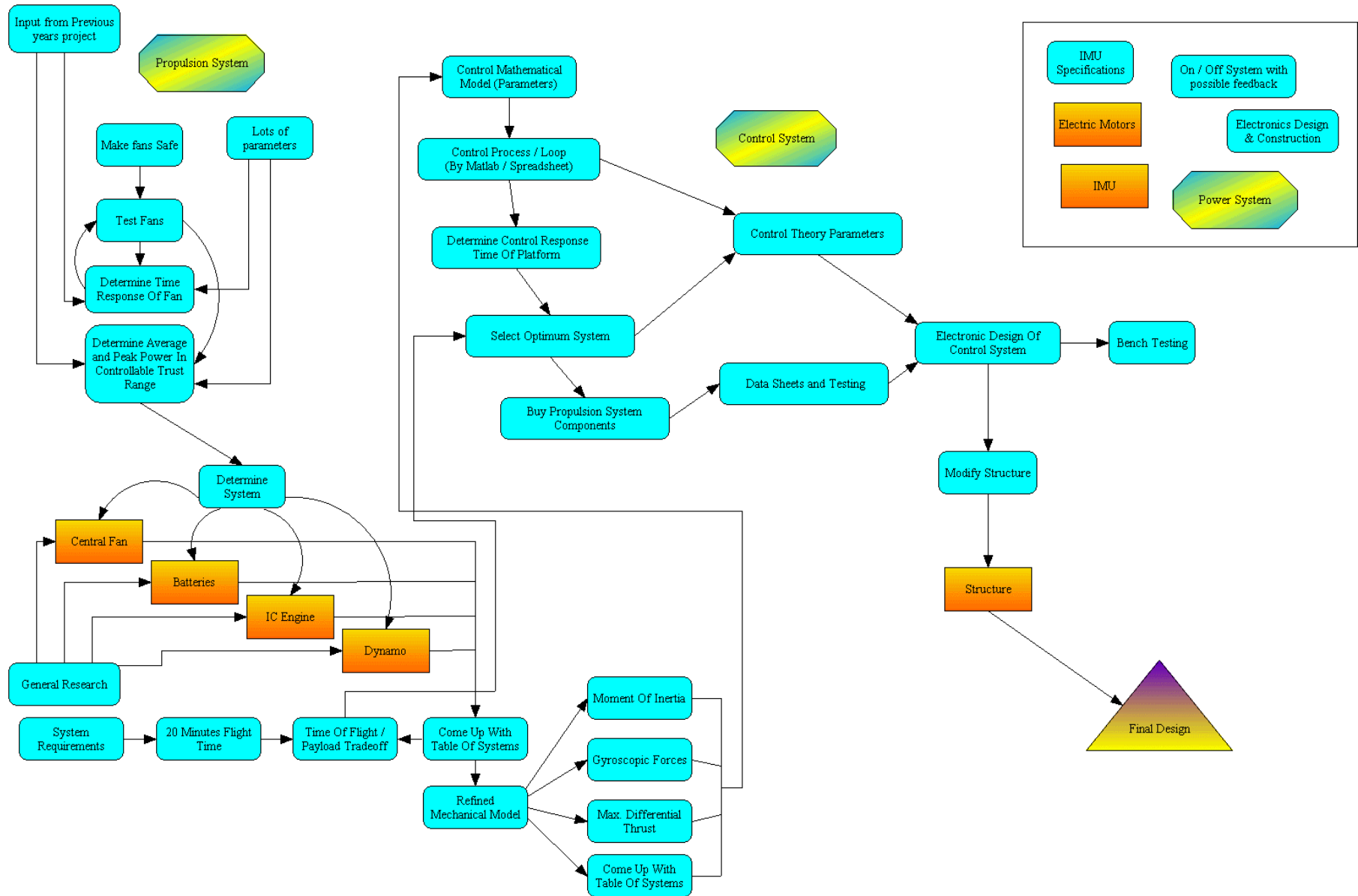


Figure 5.2. Flow of Initial Brainstorming

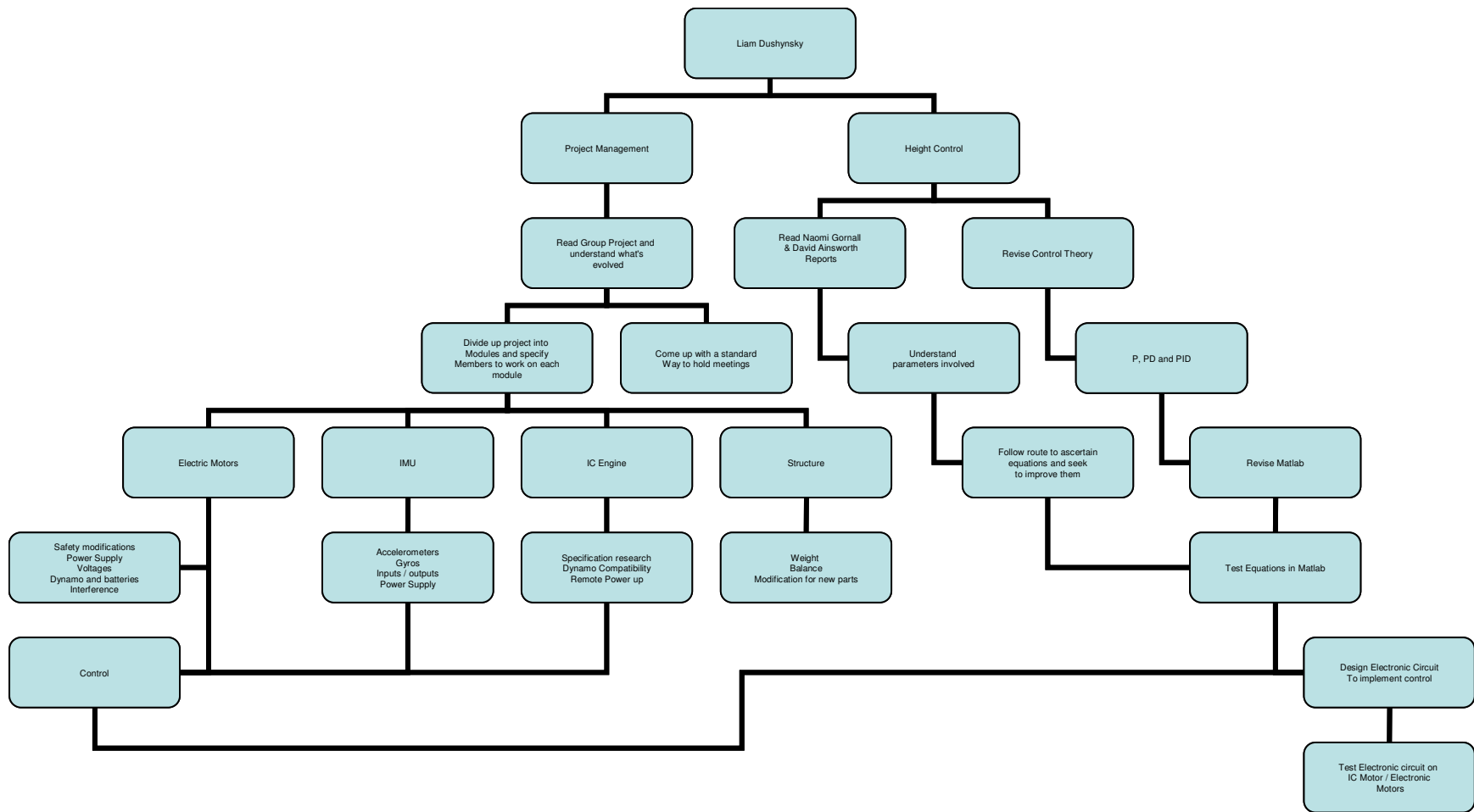


Figure 5.3. Individual Flow Chart

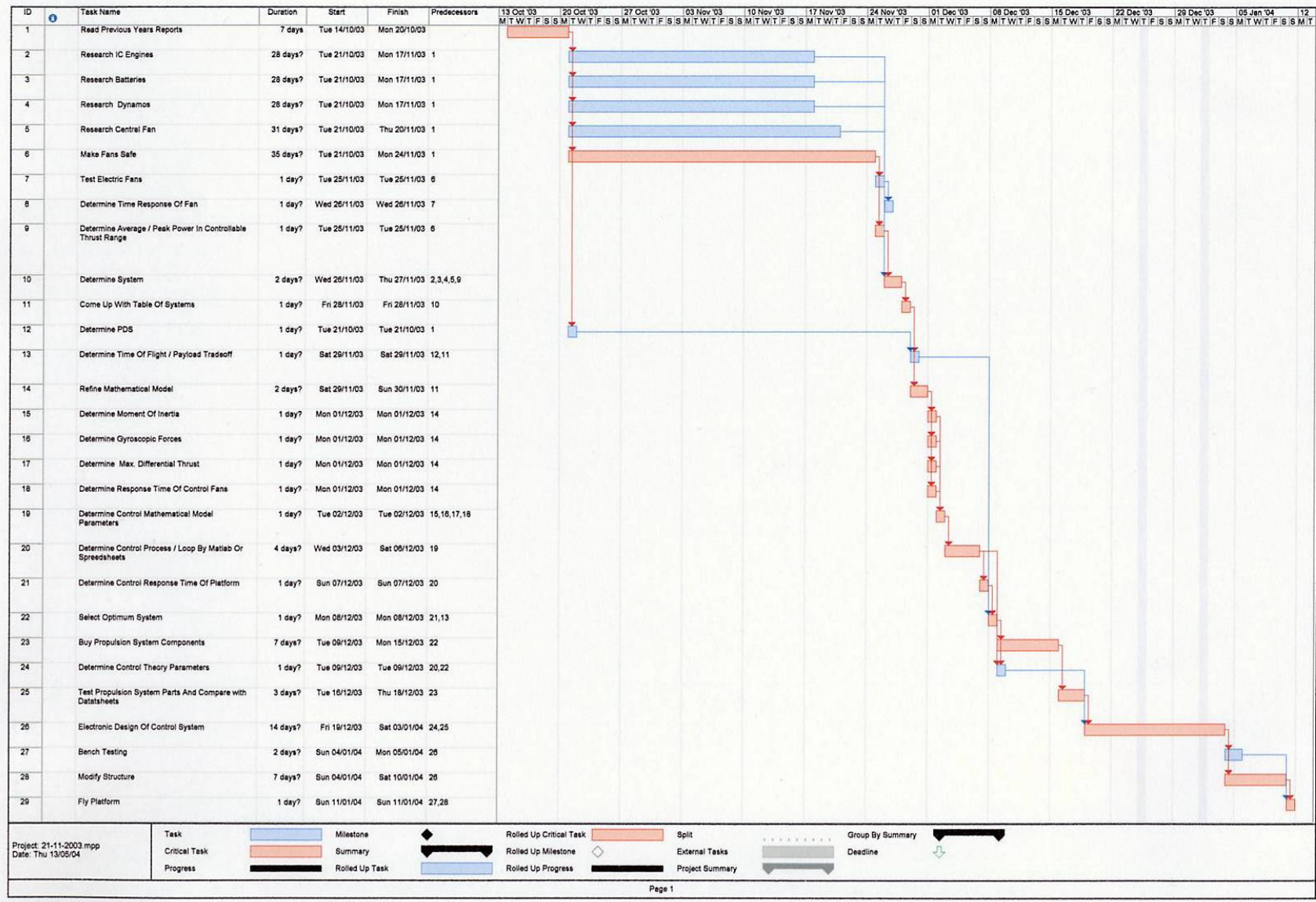


Figure 5.4. Initial Gantt Chart

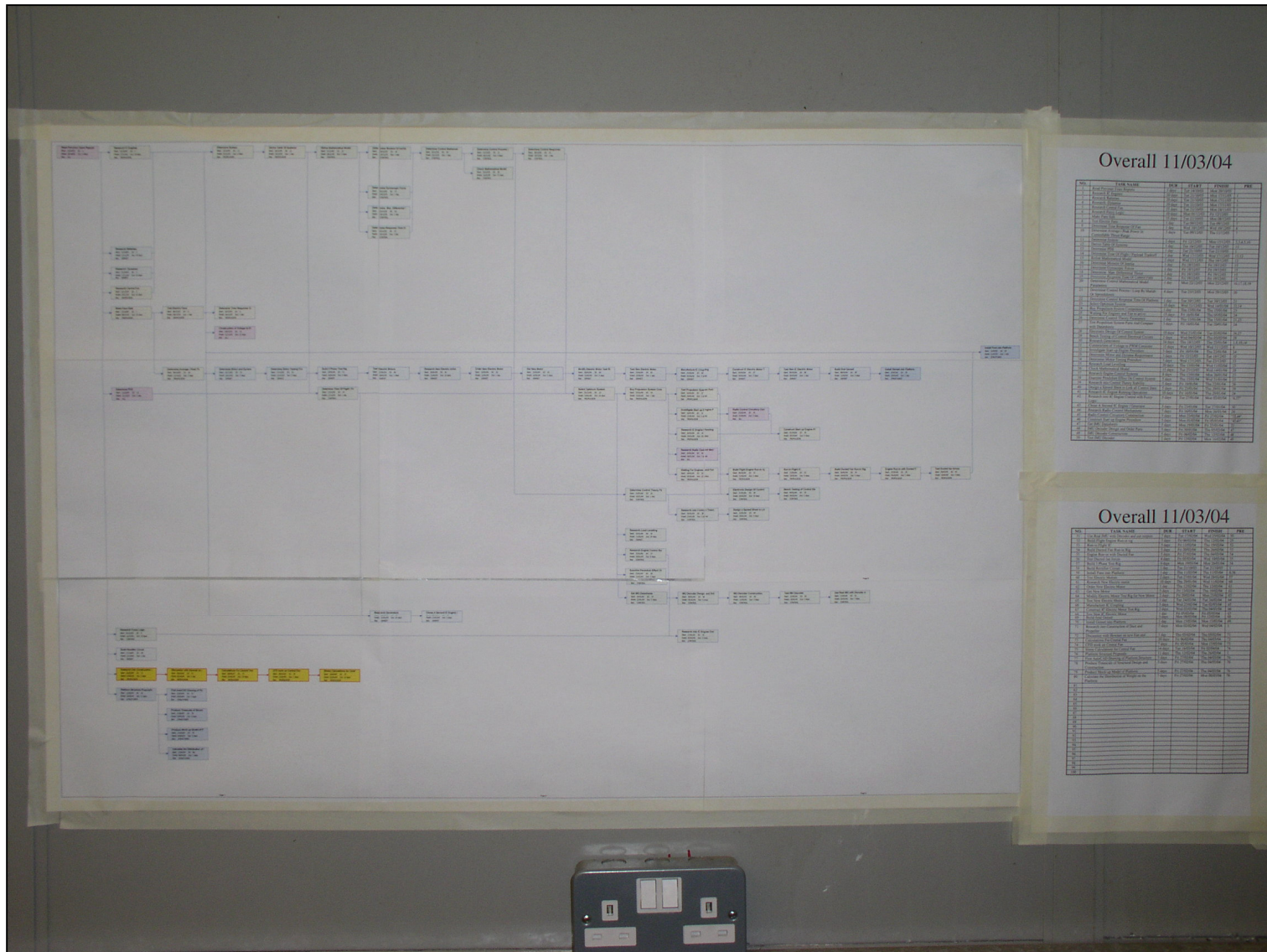


Figure 5.5. An Example of a Network Diagram

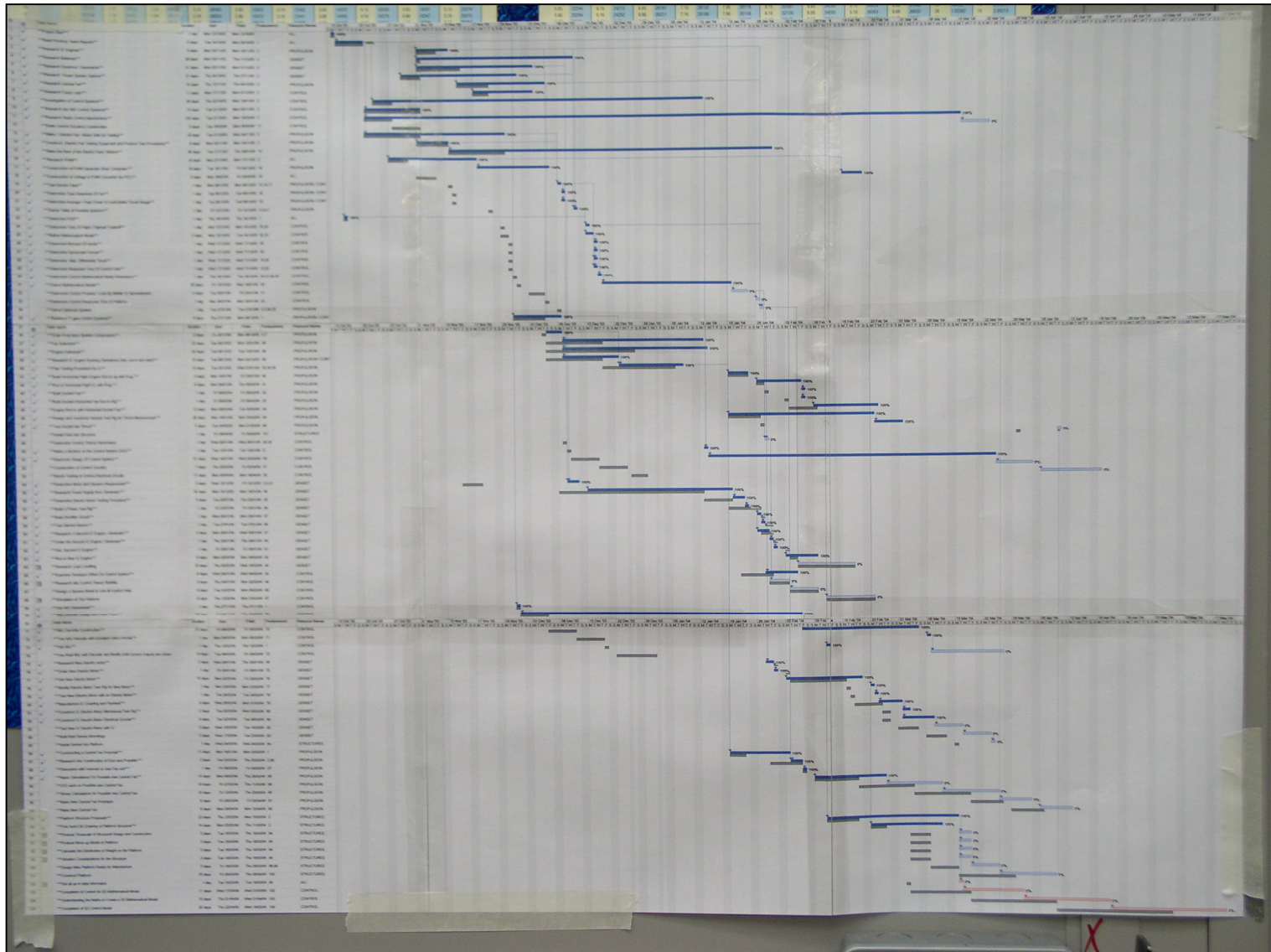


Figure 5.6. An Example of a Tracking Gantt

NO.	TASK NAME	DUR	START	FINISH	PRE
1	***Project Start***	1 day	Mon 13/10/03	Mon 13/10/03	
2	***Read Previous Years Reports***	5 days	Tue 14/10/03	Mon 20/10/03	1
3	***Research IC Engines***	6 days	Mon 03/11/03	Mon 10/11/03	2
4	***Research Batteries***	29 days	Mon 03/11/03	Thu 11/12/03	2
5	***Research Dynamos / Generators***	21 days	Mon 03/11/03	Mon 01/12/03	2
6	***Research Power System Options***	21 days	Thu 30/10/03	Thu 27/11/03	2
7	***Research Central Fan***	16 days	Thu 13/11/03	Thu 04/12/03	2
8	***Research Fuzzy Logic***	11 days	Mon 17/11/03	Mon 01/12/03	2
9	***Investigation of Control Systems***	56 days	Thu 23/10/03	Mon 12/01/04	2
10	***Research into IMU Control Systems***	10 days	Tue 21/10/03	Mon 03/11/03	2
11	***Research Radio Control Mechanisms***	103 days	Tue 21/10/03	Mon 15/03/04	2
12	***Radio Control Circuitry Construction	5 days	Tue 16/03/04	Mon 22/03/04	11
13	***Make 1 Electric Fan / Motor Safe for Testing***	25 days	Tue 21/10/03	Mon 24/11/03	2
14	***Construct Electric Fan Testing Equipment and Produce Test Procedures***	6 days	Mon 03/11/03	Mon 10/11/03	2
15	***Make the Rest of the Electric Fans / Motors***	56 days	Tue 11/11/03	Thu 29/01/04	14
16	***Research PWM***	16 days	Mon 27/10/03	Mon 17/11/03	2
17	***Construction of PWM Generator (from Computer)***	14 days	Tue 18/11/03	Fri 05/12/03	16
18	***Construction of Voltage to PWM Converter (by PIC)***	5 days	Mon 16/02/04	Fri 20/02/04	16
19	***Test Electric Fans***	1 day	Mon 08/12/03	Mon 08/12/03	"13,14,17"
20	***Determine Time Response Of Fan***	1 day	Tue 09/12/03	Tue 09/12/03	19
21	***Determine Average / Peak Power In Controllable Thrust Range***	1 day	Tue 09/12/03	Tue 09/12/03	19
22	***Derive Table of Possible Systems***	1 day	Fri 12/12/03	Fri 12/12/03	"3,4,6,7"
23	***Determine PDS***	1 day	Thu 16/10/03	Thu 16/10/03	1
24	***Determine Time Of Flight / Payload Tradeoff***	1 day	Mon 15/12/03	Mon 15/12/03	"23,22"
25	***Refine Mathematical Model***	2 days	Mon 15/12/03	Tue 16/12/03	"22,23"
26	***Determine Moment Of Inertia***	1 day	Wed 17/12/03	Wed 17/12/03	25
27	***Determine Gyroscopic Forces***	1 day	Wed 17/12/03	Wed 17/12/03	25
28	***Determine Max. Differential Thrust***	1 day	Wed 17/12/03	Wed 17/12/03	"19,25"
29	***Determine Response Time Of Control Fans***	1 day	Wed 17/12/03	Wed 17/12/03	"19,25"
30	***Determine Control Mathematical Model Parameters***	1 day	Thu 18/12/03	Thu 18/12/03	"26,27,28,29"
31	***Check Mathematical Model***	20 days	Fri 19/12/03	Mon 19/01/04	30
32	***Determine Control Process / Loop By Matlab Or Spreadsheets	4 days	Tue 20/01/04	Fri 23/01/04	31
33	***Determine Control Response Time Of Platform	1 day	Mon 26/01/04	Mon 26/01/04	32
34	***Select Optimum System	1 day	Tue 27/01/04	Tue 27/01/04	"3,7,24,33"
35	***Research Engine Control Systems***	8 days	Thu 27/11/03	Mon 08/12/03	1
36	***Order Propulsion System Components***	2 days	Fri 05/12/03	Mon 08/12/03	"3,7"
37	***Fan Delivered***	23 days	Tue 09/12/03	Mon 12/01/04	36
38	***Engine Delivered***	24 days	Tue 09/12/03	Tue 13/01/04	36
39	***Research IC Engine Running Operations (fuel, run-in and start)***	10 days	Tue 09/12/03	Mon 22/12/03	36
40	***Plan Testing Procedure for IC***	10 days	Tue 23/12/03	Wed 07/01/04	"35,36,39"
41	***Build Horizontal Flight Engine Run-in rig with Prop.***	5 days	Mon 19/01/04	Fri 23/01/04	40
42	***Run-in Horizontal Flight IC with Prop.***	9 days	Mon 26/01/04	Thu 05/02/04	41
43	***Build Ducted Fan***	1 day	Fri 06/02/04	Fri 06/02/04	42
44	***Build Ducted Horizontal Fan Run-in Rig***	1 day	Fri 06/02/04	Fri 06/02/04	42
45	***Engine Run-in with Horizontal Ducted Fan***	12 days	Mon 09/02/04	Tue 24/02/04	44
46	***Design and Construct Vertical Test Rig for Thrust Measurement***	26 days	Mon 19/01/04	Mon 23/02/04	40
47	***Test Ducted fan Thrust***	5 days	Tue 24/02/04	Mon 01/03/04	46
48	***Install Fans into Structure	1 day	Fri 09/04/04	Fri 09/04/04	101
49	***Determine Control Theory Parameters	1 day	Wed 28/01/04	Wed 28/01/04	"32,34"
50	***Make a decision on the Control System (A/D)***	1 day	Tue 13/01/04	Tue 13/01/04	9
51	***Electronic Design Of Control System***	51 days	Wed 14/01/04	Wed 24/03/04	50
52	***Construction of Control Circuitry	7 days	Thu 25/03/04	Fri 02/04/04	51

Figure 5.7. Data Input for the Analysis (part 1)

NO.	TASK NAME	DUR	START	FINISH	PRE
53	***Bench Testing of Control Electrical Circuits	11 days	Mon 05/04/04	Mon 19/04/04	52
54	***Determine Motor and Dynamo Requirement***	3 days	Wed 10/12/03	Fri 12/12/03	"3,5,21"
55	***Research Power Supply from Generator***	24 days	Mon 15/12/03	Mon 19/01/04	54
56	***Determine Electric Motor Testing Procedure***	3 days	Tue 20/01/04	Thu 22/01/04	55
57	***Build 3 Phase Test Rig***	1 day	Fri 23/01/04	Fri 23/01/04	56
58	***Build Rectifier Circuit***	1 day	Mon 26/01/04	Mon 26/01/04	57
59	***Test Electric Motors***	1 day	Tue 27/01/04	Tue 27/01/04	58
60	***Research A Second IC Engine / Generator***	3 days	Mon 26/01/04	Wed 28/01/04	57
61	***Order the Second IC Engine / Generator***	1 day	Thu 29/01/04	Thu 29/01/04	60
62	***Get Second IC Engine***	1 day	Fri 30/01/04	Fri 30/01/04	61
63	***Run-in New IC Engine***	6 days	Mon 02/02/04	Mon 09/02/04	62
64	***Research Load Levelling	10 days	Thu 05/02/04	Wed 18/02/04	34
65	***Examine Pendulum Effect On Control System***	6 days	Wed 28/01/04	Wed 04/02/04	34
66	***Research into Control Theory Stability	3 days	Thu 29/01/04	Mon 02/02/04	49
67	***Design a Spreed Sheet to Link all Control Data	5 days	Tue 03/02/04	Mon 09/02/04	66
68	***Simulation of The Platform	8 days	Thu 12/02/04	Mon 23/02/04	67
69	***Get IMU Datasheets***	1 day	Thu 27/11/03	Thu 27/11/03	1
70	***IMU Decoder Design and Order Parts***	48 days	Fri 28/11/03	Thu 05/02/04	69
71	***IMU Decoder Construction***	21 days	Fri 06/02/04	Fri 05/03/04	70
72	***Test IMU Decoder with Emulator Until it Works***	1 day	Mon 08/03/04	Mon 08/03/04	71
73	***Get IMU***	1 day	Thu 12/02/04	Thu 12/02/04	1
74	***Use Real IMU with Decoder and Modify Until Correct Outputs are Given	14 days	Tue 09/03/04	Fri 26/03/04	72
75	***Research New Electric motor***	2 days	Wed 28/01/04	Thu 29/01/04	59
76	***Order New Electric Motor***	1 day	Fri 30/01/04	Fri 30/01/04	75
77	***Get New Electric Motor***	15 days	Mon 02/02/04	Fri 20/02/04	76
78	***Modify Electric Motor Test Rig for New Motor***	1 day	Mon 23/02/04	Mon 23/02/04	77
79	***Test New Electric Motor with an Electric Motor***	1 day	Tue 24/02/04	Tue 24/02/04	78
80	***Manufacture IC Coupling and Flywheel***	4 days	Wed 25/02/04	Mon 01/03/04	79
81	***Construct IC Electric Motor Mechanical Test Rig***	2 days	Tue 02/03/04	Wed 03/03/04	80
82	***Construct IC Electric Motor Electrical Circuits***	6 days	Tue 02/03/04	Tue 09/03/04	80
83	***Test New IC Electric Motor with IC	5 days	Wed 10/03/04	Tue 16/03/04	82
84	***Build final Genset Mountings	5 days	Wed 17/03/04	Tue 23/03/04	83
85	***Install Genset into Platform	1 day	Wed 24/03/04	Wed 24/03/04	84
86	***Constructing a Central Fan Proposal***	11 days	Mon 19/01/04	Mon 02/02/04	1
87	***Research into Construction of Duct and Propeller***	3 days	Tue 03/02/04	Thu 05/02/04	"2,86"
88	***Discussion with Howmet on new Fan unit***	1 day	Fri 06/02/04	Fri 06/02/04	87
89	***Basic Calculations For Possible new Central Fan***	14 days	Mon 09/02/04	Thu 26/02/04	88
90	***CFD work on Possible new Central Fan	10 days	Fri 27/02/04	Thu 11/03/04	89
91	***Stress Calculations for Possible new Central Fan	10 days	Fri 12/03/04	Thu 25/03/04	90
92	***Make New Central Fan Prototype	6 days	Fri 26/03/04	Fri 02/04/04	91
93	***Make New Central Fan	6 days	Mon 05/04/04	Mon 12/04/04	92
94	***Platform Structure Proposals***	23 days	Thu 12/02/04	Mon 15/03/04	2
95	***First AutoCAD Drawing of Platform Structure***	14 days	Mon 23/02/04	Thu 11/03/04	2
96	***Produce Timescale of Structural Design and Construction	3 days	Tue 16/03/04	Thu 18/03/04	94
97	***Produce Mock-up Model of Platform	3 days	Tue 16/03/04	Thu 18/03/04	94
98	***Calculate the Distribution of Weight on the Platform	3 days	Tue 16/03/04	Thu 18/03/04	94
99	***Vibration Considerations for the Structure	3 days	Tue 16/03/04	Thu 18/03/04	94
100	***Design New Platform Ready for Manufacture	5 days	Fri 19/03/04	Thu 25/03/04	"98,99"
101	***Construct Platform	10 days	Fri 26/03/04	Thu 08/04/04	100
102	***Get all up-to-date informaion	1 day	Tue 16/03/04	Tue 16/03/04	94
103	***Completion of Control for 2D Mathematical Model	11 days	Wed 17/03/04	Wed 31/03/04	102
104	***Understanding the Maths to Create a 3D Mathematical Model	15 days	Thu 01/04/04	Wed 21/04/04	103
105	***Completion of 3D Control Model	20 days	Thu 22/04/04	Wed 19/05/04	104
106	***Fly Platform	1 day	Thu 20/05/04	Fri 21/05/04	"95,103,105"

Figure 5.7. Data Input for the Analysis (part 2)

Appendix 6

Engine “Run-in” Instructions

- エンジンの運転中は、顔や身体の一部をプロペラ回転面より前へは絶対に出さないでください。
 - ① まずエンジンを丈夫なテストベンチに取り付けます。直径12インチ以上で、中央部の強度が十分ある木製プロペラの両端を切り、直径が10インチ前後になるようにして、最高回転が16,000〜18,000回転になるようなプロペラを作ります。プロペラを取り付け開始します。実際に使用する燃料を使用し、少くとも最初の20分は濃い目の混合気で運転します。その後は10分毎にニードルバルブを絞り、徐々に回転を上げながら最高回転になるまで運転を続け、十分なブレイクインを行います。
 - ② 次にエンジンを機体に搭載し始動します。地上でニードルバルブを絞っていき最高回転になるのを確認してから約1/2回転戻します。混合気が濃くなった事を確認してから飛行に入ります。(ニードルバルブの戻す回数は、燃料タンクとキャブレターまでの距離、燃料の種類、チューンドサイレンサーの長さ等によって変わります)
 - ③ 最適なニードルバルブセッティングで、エンジンがオーバーヒートしてパワーが落ちたりせず、順調に運転できるようになったら、高ニトロメタン燃料を使ってもよいでしょう。しかし、ニトロメタンの含有量を増加させるたびに、最初の運転位置よりかなり濃い目のニードルセッティングから始めて、②の操作をしてください。
- (注意) 地上でのブレイクインでもかなりの高速回転になりますので、テストベンチやプロペラの強度には十分注意してください。

サイレンサー

本エンジンは、チューンドサイレンサーの使用を前提に作られています。使用方法については、サイレンサーメーカーの取扱説明書を参照してください。

キャブレター

本エンジンには、別紙記載の9B型キャブレターが装備されています。キャブレターの調整は、別紙キャブレター取扱説明書を必ずお読みいただき、その性能が十分発揮できるよう正しく調整してください。

アフターサービス

◆エンジンの修理について

- よく洗浄してエンジン本体のみを弊社「OSエンジンサービス係」までお送りください。(エンジン以外のものが付いていたり汚れがひどいと分解や洗浄に時間がかかり、修理代が高くなります) この時、故障時の状態及び修理希望事項を必ずお書き添えください。
- 原則として弊社到着後10日以内で修理完了致します。なお修理品は修理の内容及び注意事項を書いた修理カードを添えてご返送いたします。
- 修理品のお支払いについては、コレクトサービス(代金支払いシステム)により発送させていただきますので、お届けした際に修理代金および送料をお支払いください。

◆交換部品について

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重量	50g	75g	100g	150g	200g	250g	500g	750g	1Kg	2Kg
料金	120円	140円	160円	200円	240円	270円	390円	580円	700円	950円

送料は平成11年3月現在で、法規改正などにより変更になる場合があります。

- rpm at approximately 10 minute intervals, until the engine runs freely at high speed without loss of power. Take care not to lean out the mixture too far: this will cause over-heating and loss of power.
- 2) Using the same test propeller, but now with the fuel that you intend to employ for normal flying, run the engine again, following the procedure as outlined in paragraph (1) above.
- 3) Now install the engine in your model. Use the fuel that you intend to employ for normal flying. For the first flight, set the needle-valve as follows. Close the needle-valve gradually until maximum rpm are reached, then open the needle-valve approximately 1/2 turn. (The exact setting of the needle-valve depends on the distance between the needle-valve and the fuel tank, type of fuel, tuned silencer length, etc.) Fly the model only after making sure that the mixture has become rich. Then, with each successive run, gradually and progressively close the needle setting for increased rpm. Keep the needle-valve on the rich side for the first 5 or 10 flights and avoid steep climbing or extended periods of nose-up flying during this period.
- 4) When the engine is capable of running at the optimum performance setting without overheating or loss of power, a fuel having a higher nitromethane content may be tried if extra power is being sought. However, each time the nitromethane percentage is increased, always take the precaution of making a trial run with a rich needle setting.

SILENCER

As this engine has been designed primarily for use with a tuned length exhaust silencer system, a conventional silencer is not supplied. Select a silencer suitable for use with the ducted-fan unit chosen, referring to the instructions supplied with the fan unit.

CARBURETTOR

This engine is equipped, as standard, with the special O.S. Type 9B automatic carburettor described in the attached instruction sheet. An exhaust pressurized fuel system should be used for best results.

GUARANTEE

This engine is constructed from the very best materials available and to the very highest engineering standards, using the most advanced precision machinery. However, the extremely high stresses imposed by high-speed ducted fan operation which are exacerbated by the use of powered fuels containing very high concentrations of nitromethane, plus the considerable risks from minute particles of foreign matter being drawn into the duct on the flying-field, constitute hazards which are beyond a manufacturer's control. Accordingly, we regret that it is not possible to extend our usual warranty terms to this particular engine - i.e. no guarantee is offered against material wear, or damage resulting therefrom, in actual use.

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部 品 表 PARTS RIST

品 名	Description	品名コード Code No.		
		65VR-DFABC	91VR-DF	91VR-DF (Round Head)
クランクケース	Crankcase	27201001(5800)	27501001(5800)	27501001(5800)
フロント・ハウジング	Front Housing		27501600(2100)	
リヤ・ハウジング	Rear Housing		27501801(3000)	
クランクシャフト	Crankshaft	27202020(3700)		27502000(4000)
シリンダー・ピストン 一式	Cylinder & Piston Assy	27203010(11000)		27503000(11000)
ヒートシンク・ヘッド	Heat Sink Head		27504000(3200)	
シリンダー・ヘッド	Cylinder Head	27204030(3200)		27504010(3200)
コネクティング	Connecting Rod	27205001(1300)		27505001(1700)
ピストン・ピン	Piston Pin	27106007(480)		27506000(550)
ピストン・ピン・リテーナー	Piston Pin Retainer	26617004(130)		27517000(130)
ドライブ・ワッシャー(ウッドラフ・キー付)	Drive Hub (with Woodruff key)		27508000(750)	
ウッドラフ・キー	Woodruff Key		29008219(110)	
プロペラ・ワッシャー	Propeller Washer		28009002(160)	
プロペラ・ナット	Propeller Nut		45010002(100)	
スクリュー・セット	Screw Set		27213008(530)	
ガスケット・セット	Gasket Set	27214000(200)		27514000(200)
スラスト・ワッシャー	Thrust Washer		46120000(110)	
リヤ・ローター	Rear Rotor		27516000(2400)	
クランクシャフト・ベアリング (前)	Crankshaft Ball Bearing (Front)		26731002(750)	
クランクシャフト・ベアリング (後)	Crankshaft Ball Bearing (Rear)		27330010(1200)	
キャブレター・スロットル (9B)	Carburettor Throttle (Type 9B)		29381010(6300)	
リモート・ニードル	Remote Needle Valve Assy	*28282000(2100)		28282000(2100)
エキゾースト・アダプター (No.4)	Exhaust Adaptor (No.4)		27326100(1600)	
グロープラグNo.8	Glowplug No.8		71608001(480)	
シリコン・シール・リング	Silicone Seal Ring		27126258(440)	

● 印オプション Optional extra

本仕様は製品改良のため予告なく変更することがあります。
The specifications are subject to alteration for improvement without notice.

O.S. エンジン
小川精機株式会社
〒546-0003 大阪市東住吉区今川13丁目6番15号
電話 (06) 6702-0225 番(代)
FAX (06) 6704-2722 番

O.S. ENGINES MFG.CO.LTD.
6-15 3-Chome Imagawa Higashiumiyoshi-ku
Osaka 546-0003, Japan TEL. (06)6702-0225
FAX. (06)6704-2722

Appendix 7

Propulsion Test

Results

Date	Thrust	Strobe	RPM	Comments	Date	Thrust	Strobe	RPM	Comments
27/02/2004	4.1	100	20000	no duct	04/05/2004	4.645	97	19400	duct 3
01/03/2004	1.34	60	12000	no duct		4.145	100	20000	duct 3
	3.9	100	20000	no duct		4.145	99	19800	duct 3
	4	104	20800	no duct		4.345	102	20400	duct 5
09/03/2004	3.8	100	20000	no duct		4.245	96	19200	duct 4
10/03/2004	3.46	96	19200	no duct		3.345	100	20000	no duct
	2.94	82	16400	no duct		3.62	102	20400	-4
	3.7	99	19800	no duct		3.4	98	19600	-8
	3.2	90	18000	no duct		3.2	96	19200	-2
	3.5	96	19200	no duct		3.53	100	20000	2
	3	87	17400	no duct		3.73	102	20400	4
	3.63	100	20000	no duct		3.82	103	20600	8
	3.2	92	18400	no duct		3.94	102	20400	6
	3.7	98	19600	no duct		3.26	100	20000	0
	3.8	100	20000	no duct	06/05/2004	3.72	100	20000	no duct
16/03/2004	2.5	98	19600	no duct		3.76	100	20000	no duct
	2.8	104	20800	no duct		3.95	99	19800	duct 5
	2.65	100	20000	no duct		4.4	100	20000	duct 5
	0.6	49	9800	no duct		4.35	102	20400	duct 5
	2.475	91	18200	no duct		4.52	100	20000	duct 4
	2.9	99	19800	no duct		4.55	101	20200	duct 4
18/03/2004	2.8	98	19600	cardboard test 3		4.26	97	19400	duct 3
	3.1	100	20000	cardboard test 4		3.335	99	19800	duct 1
	3.3	100	20000	cardboard test 4	14/05/2004	0.855	50	10000	no duct
	3.6	99	19800	cardboard test 4		0.705	50	10000	no duct
19/03/2004	3.8	100	20000	no duct		1.245	61	12200	no duct
22/03/2004	3.8	100	20000	top and bottom duct		2.335	80	16000	no duct
23/03/2004	4.3	100	20000	both ducts		0.34	33	6600	no duct
	3.4	100	20000	bottom duct only		0.58	41	8200	no duct
	4.6	100	20000	duct 2		0.95	50	10000	no duct
	4	100	20000	no duct		1.335	60	12000	no duct
27/03/2004	4.8	100	20000	duct 1		1.68	67	13400	no duct
	5.1	100	20000	duct 4		2.5	81	16200	no duct
						3.63	99	19800	no duct
						1.57	68	13600	no duct

Note: This data is the collaboration of all the propulsion test results and was compiled by R. Holbrook

Appendix 8 Shift Register Datasheet

Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/9309.pdf>

Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I _{pin} /I _L	Output I _{pin} /I _{OL}
A, B	Data Inputs	1.0/1.0	20 μ A/-0.6 mA	20 μ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/-0.6 mA	20 μ A/-0.6 mA
MR	Master Reset Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA	20 μ A/-0.6 mA
Q ₀ -Q ₇	Outputs	50/33.3	-1 mA/20 mA	-1 mA/20 mA

Functional Description

The 74F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q₀ the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

Operating Mode	Inputs		Outputs	
	MR	A B	Q ₀	Q ₁ -Q ₇
Reset (Clear)	L	X X	L	L-L
Shift	H	L L	L	Q ₀ -Q ₆
	H	H H	L	Q ₀ -Q ₆
Shift	H	L L	L	Q ₀ -Q ₆
	H	H H	L	Q ₀ -Q ₆

H(H) = HIGH Voltage Levels
L(L) = LOW Voltage Levels
X = Immaterial

Φ = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

74F164A

www.fairchildsemi.com

74F164A Serial-In, Parallel-Out Shift Register

October 1989
Revised August 1999

FAIRCHILD SEMICONDUCTOR™

74F164A
Serial-In, Parallel-Out Shift Register

General Description

The 74F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The other input to the AND gate is the Master Reset which also is asynchronous with the clock. The 74F164A is a faster version of the 74F164.

Features

- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 74F164A is a faster version of the 74F164.

Ordering Code:

Order Number	Package Number	Package Description
74F164ASC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F164ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F164AFC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tube and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

Connection Diagram


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Appendix 9

DAC Datasheet

Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/1846.pdf>



BURR-BROWN
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DAC712

16-BIT DIGITAL-TO-ANALOG CONVERTER
With 16-Bit Bus Interface

DESCRIPTION

DAC712 is a complete 16-bit resolution D/A converter with 16 bits of monotonicity over temperature.

DAC712 has a precision $\pm 10\%$ temperature compensated voltage reference, $\pm 10\%$ output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to bipolar zero.

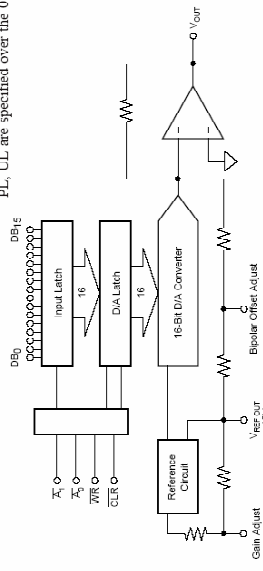
GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC712 is available in two linearity error performance grades: $\pm 4LSB$ and $\pm 2LSB$ and three differential linearity grades: $\pm 4LSB$, $\pm 2LSB$, and $\pm 1LSB$. The DAC712 is specified at power supply voltages of $\pm 12V$ and $\pm 15V$.

DAC712 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. The DAC712P U, PB, UB, are specified over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range and the DAC712PK, UK, PL, UL are specified over the $0^{\circ}C$ to $+70^{\circ}C$ range.

FEATURES

- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: $\pm 10V$
- 13-, 14-, AND 15-BIT LINEARITY GRADES
- 16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES



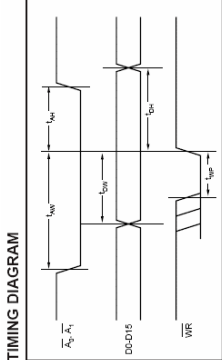
International Airport Industrial Park • Mailing Address: 20 Box 11060, Tucson, AZ 85714 • Street Address: 6750 S. Tucson Blvd., Tucson, AZ 85716 • Tel: (520) 746-1111 • Fax: (520) 746-1111
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ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V, $+17V$
$-V_{CC}$ to COMMON	0V, $-17V$
Digital Inputs to COMMON	$-1V$ to $+V_{CC}$ $-0.7V$
External Voltage Applied to BFO and Range Resistors	$-1V$ to $+V_{CC}$ $-0.7V$
Input Pins Short to COMMON	Indefinite
Power Dissipation	750mW
Storage Temperature	$-60^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
DAC712P	Plastic DIP	246
DAC712U	Plastic SOIC	217
DAC712PB	Plastic DIP	246
DAC712PK	Plastic DIP	246
DAC712UK	Plastic SOIC	217
DAC712PL	Plastic SOIC	217
DAC712UL	Plastic SOIC	217

TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{WR}	Data Valid to End of WR	50	50	ns
t_{WH}	A_1, A_2 Valid to End of WR	50	50	ns
t_{DWH}	A_1, A_2 Hold after End of WR	10	10	ns
t_{DHL}	Data Hold after end of WR	10	10	ns
t_{WPH}	Write Pulse Width	50	50	ns
t_{CLR}	CLEAR Pulse Width	200	200	ns

NOTES: (1) For single-buffered operation, t_{WR} is 80ns min. Refer to page 10.

ORDERING INFORMATION

PRODUCT	TEMPERATURE RANGE	LINEARITY ERROR MAX at $+25^{\circ}C$	DIFFERENTIAL LINEARITY ERROR MAX at $+25^{\circ}C$
DAC712P	$-40^{\circ}C$ to $+85^{\circ}C$	$\pm 4LSB$	$\pm 4LSB$
DAC712U	$-40^{\circ}C$ to $+85^{\circ}C$	$\pm 4LSB$	$\pm 4LSB$
DAC712PB	$-40^{\circ}C$ to $+85^{\circ}C$	$\pm 2LSB$	$\pm 2LSB$
DAC712UB	$-40^{\circ}C$ to $+85^{\circ}C$	$\pm 2LSB$	$\pm 2LSB$
DAC712PK	$0^{\circ}C$ to $+70^{\circ}C$	$\pm 2LSB$	$\pm 2LSB$
DAC712UK	$0^{\circ}C$ to $+70^{\circ}C$	$\pm 2LSB$	$\pm 2LSB$
DAC712PL	$0^{\circ}C$ to $+70^{\circ}C$	$\pm 1LSB$	$\pm 1LSB$
DAC712UL	$0^{\circ}C$ to $+70^{\circ}C$	$\pm 1LSB$	$\pm 1LSB$

TRUTH TABLE

A_1	A_2	WR	CLR	DESCRIPTION
0	1	1	0	Load Input Latch
1	0	1	0	Load D/A Latch
1	1	0	0	No Change
0	0	0	0	Latches Transparent
X	X	X	1	No Change
X	X	X	0	Repeat D/A Latch

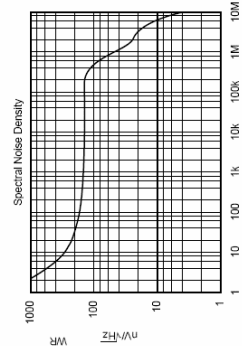
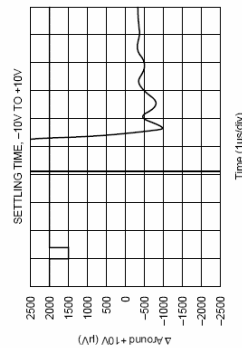
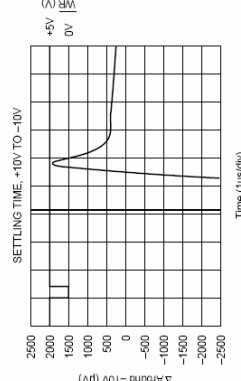
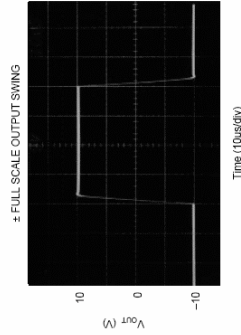
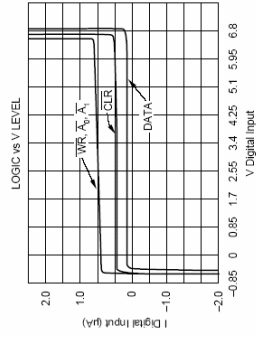
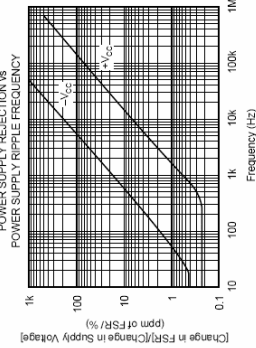
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

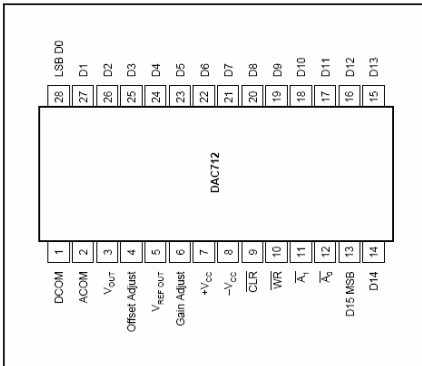
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.



PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Power Supply return for digital currents.
2	ACOM	Analog Supply Return.
3	V _{out}	±10V/DIA Output.
4	Off Adj	Offset Adjust (Bipolar).
5	V _{ref out}	Voltage Reference Output.
6	Gain Adj	Gain Adjust.
7	+V _{CC}	+12V to +15V Supply.
8	-V _{CC}	-12V to -15V Supply.
9	CLR	CLEAR Sets DIA output to BIPOLAR ZERO (Active Low).
10	WR	Write (Active Low).
11	A ₁	Address for Data Bit 14 (Active Low).
12	A ₀	Address for Data Bit 13 (Active Low).
13	D15	Enable for Data Bit 15 (Active Low).
14	D14	Data Bit 15 (Most Significant Bit).
15	D13	Data Bit 14.
16	D12	Data Bit 13.
17	D11	Data Bit 12.
18	D10	Data Bit 11.
19	D9	Data Bit 10.
20	D8	Data Bit 9.
21	D7	Data Bit 8.
22	D6	Data Bit 7.
23	D5	Data Bit 6.
24	D4	Data Bit 5.
25	D3	Data Bit 4.
26	D2	Data Bit 3.
27	D1	Data Bit 2.
28	D0	Data Bit 0 (Least Significant Bit).

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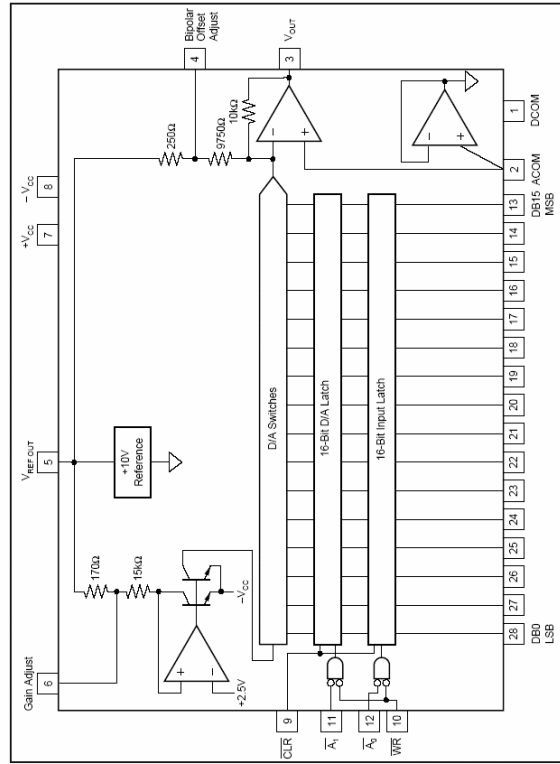


FIGURE 1. DAC712 Block Diagram.

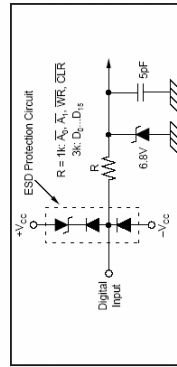


FIGURE 2. Equivalent Circuit of Digital Inputs.

OUTPUT VOLTAGE SWING

The output amplifier of DAC712 is committed to a ±10V output range. DAC712 will provide a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

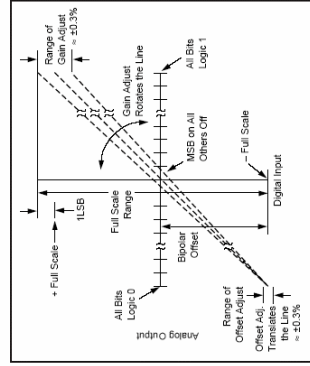


FIGURE 3. Relationship of Offset and Gain Adjustments.

Offset Adjustment

Apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for -10V.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC712 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

DAC712 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched. The CLR input resets both the input latch and the D/A latch to give a bipolar zero output.

LOGIC INPUT COMPATIBILITY

DAC712 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic "0" and control inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC712 is designed to accept positive-true binary two's complement (BTC) input codes which are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of 7FFF_{HEX} gives a plus full scale output, 8000_{HEX} gives a minus full scale output, and 0000_{HEX} gives bipolar zero output.

INTERNAL REFERENCE

DAC712 contains a +10V reference. The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than -1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC712 is guaranteed over the specification temperature range to 13, 14, 15, and 16 bits for performance grades DAC712P/U, DAC712PB/UB, DAC712PK/UK, and DAC712PL/UJ, respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry (FFFF_{HEX} to 0000_{HEX} and 0000_{HEX} to FFFF_{HEX}; BTC codes) the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_s .

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power, in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_s .

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from 7FFF_{HEX} to 8000_{HEX}.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC712 output amplifier is connected internally for the ±10V bipolar (20V) output range. That is, the bipolar offset resistor is connected to an internal reference voltage and the 20V range resistor is connected internally to V_{OUT}. DAC712 cannot be connected by the user for unipolar operation.

DIGITAL INTERFACE

BUS INTERFACE
DAC712 has 16-bit double-buffered data bus interface with control lines for easy interface to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.

there is no change in DAC712 ACOM current, provided that R₃ is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC712 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

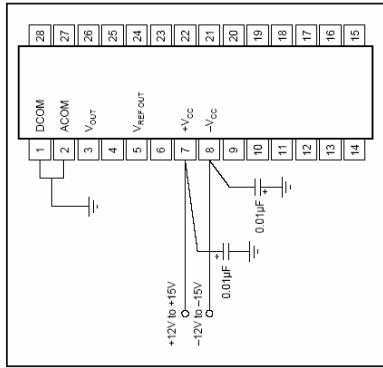


FIGURE 4. Power Supply Connections.

critical settling time may be able to use 0.01µF at -V_{CC} as well as at +V_{CC}. The capacitors should be located close to the package.

DAC712 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes. Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package. If several DAC712s are used or if DAC712 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and V_{REF} OUT is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R₁ through R₃. As long as the load resistance R₂ is constant, R₁ simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R₂ is part of R₁ if the output voltage is sensed at ACOM. In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because

the SYSTEM GROUND point is reasonable, because

DAC712 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 30µV	
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BITC	DESCRIPTION
7FFF _H	+ Full Scale - 1LSB +5.999995
4000 _H	3/4 Scale -5.000000
0001 _H	BPZ + 1LSB -0.000305
0000 _H	Bipolar Zero (BPZ) 0.000000
FFFF _H	BPZ - 1LSB -0.000305
CD00 _H	1/4 Scale -5.000000
8000 _H	Minus Full Scale -10.000000

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milli-inches long wide printed circuit conductor 60 milli-inches long will result in a voltage drop of 150µV.

The analog output of DAC712 has an LSB size of 305µV (-90dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC712's noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at -V_{CC}. Applications with less

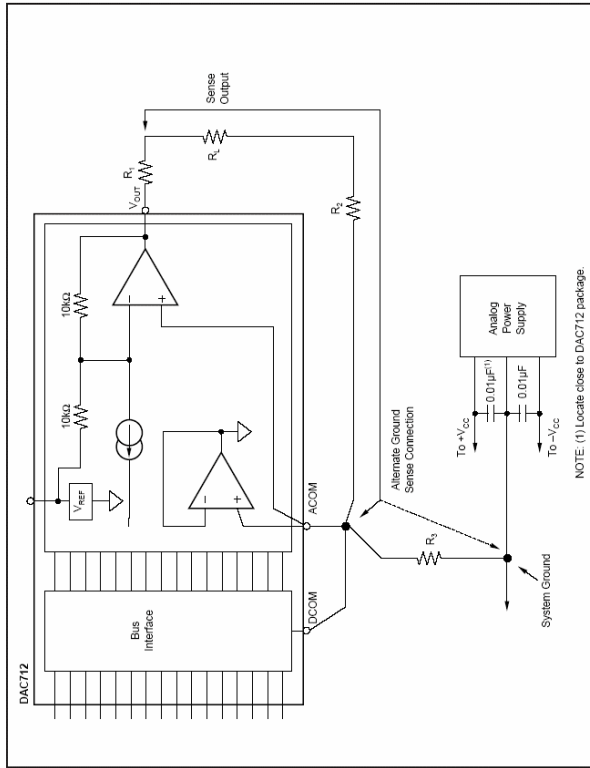


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

\overline{A}_0 is the enable control for the DATA INPUT LATCH \overline{A}_1 is the enable for the D/A LATCH. \overline{WR} is used to strobe data into latches enabled by \overline{A}_0 and \overline{A}_1 . Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

CLR sets the INPUT DATA LATCH to all zero and the D/A LATCH to a code that gives bipolar 0V at the D/A output.

SINGLE-BUFFERED OPERATION

To operate the DAC712 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting \overline{A}_0 to DCOM. If \overline{A}_1 is not used to enable the

D/A, it should be connected to DCOM also. For this mode of operation, the width of \overline{WR} will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

TRANSPARENT INTERFACE

The digital interface of the DAC712 can be made transparent by asserting \overline{A}_0 , \overline{A}_1 , and \overline{WR} LOW, and asserting CLR HIGH.

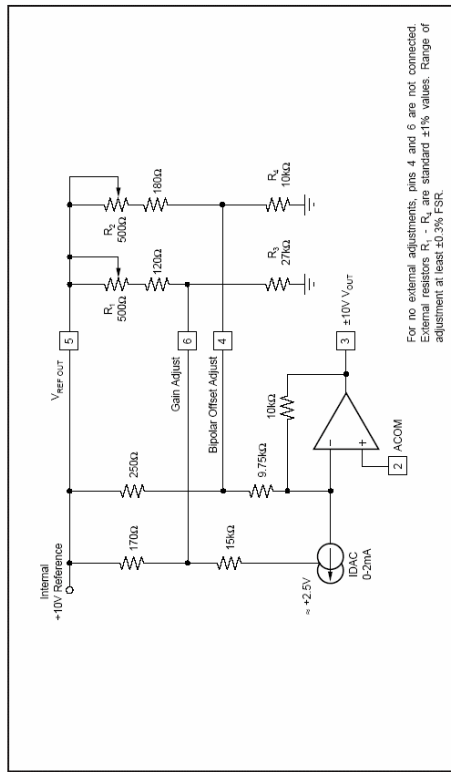


FIGURE 6. Manual Offset and Gain Adjust Circuits.

Appendix 10

4-16 Decoder

Datasheet

Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/9592.pdf>

CD4514BC • CD4515BC

CD4514BC • CD4515BC 4-Bit Latched/4-to-16 Line Decoders

October 1987
Revised January 1999

FAIRCHILD SEMICONDUCTOR™

CD4514BC • CD4515BC

4-Bit Latched/4-to-16 Line Decoders

www.fairchildsemi.com

General Description

The CD4514BC and CD4515BC are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514BC (output active high option) presents a logical "1" at the selected output, whereas the CD4515BC presents a logical "0" at the selected output. The input latches are R-S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL fan out of 2 compatibility: driving 74L
- Low quiescent power dissipation: 0.025 µW/package @ 5.0 V_{CC}
- Single supply operation
- Input impedance = 10¹² Ω, typically
- Plug-in replacement for MC14514, MC14515

Ordering Code:

Order Number	Package Number	Package Diagram
CD4514BCWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4514BCN	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
CD4515BCWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4515BCN	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Devices also available in "Tube and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for SOIC and DIP

Top View

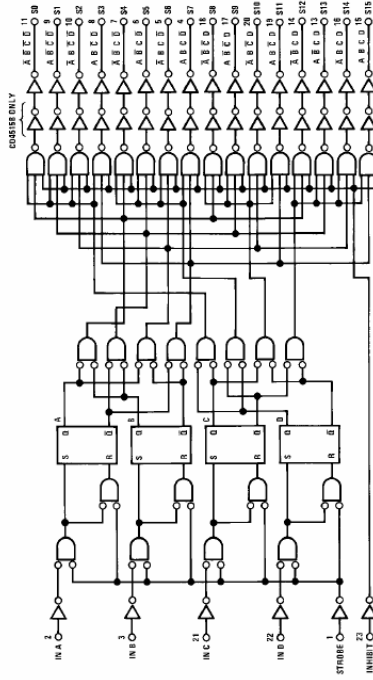
Truth Table

Decode Truth Table (Strobe = 1)

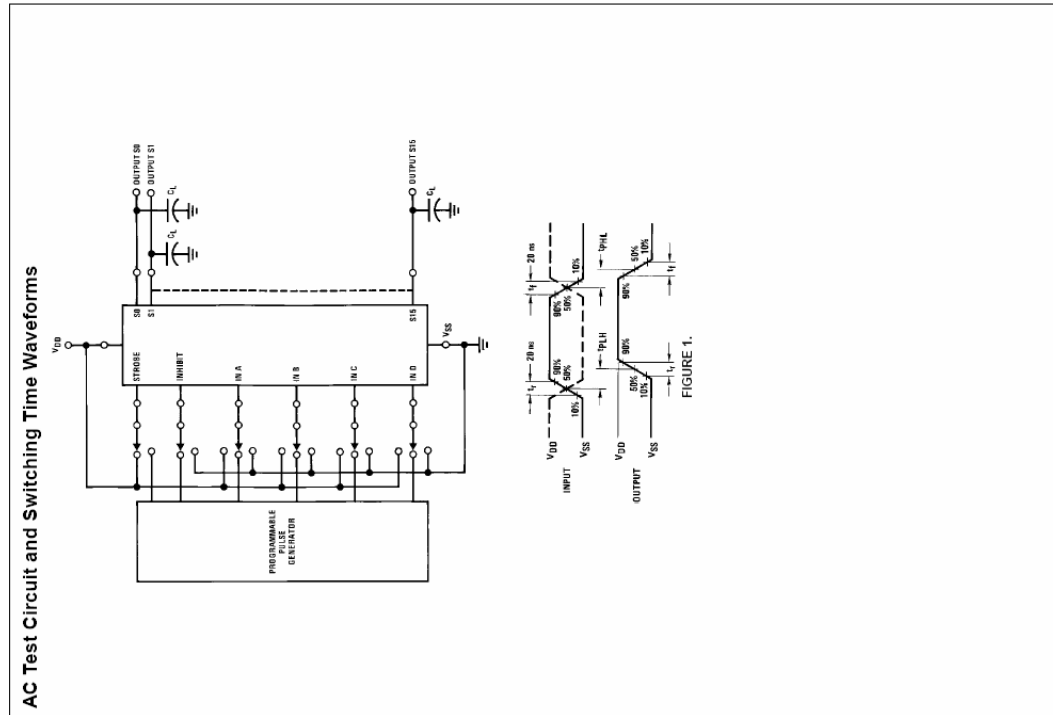
Inhibit	Data Inputs				Selected Output	
	D	C	B	A	CD4514 = Logic "1"	CD4515 = Logic "0"
0	0	0	0	0	S0	
0	0	0	0	1	S1	
0	0	0	1	0	S2	
0	0	0	1	1	S3	
0	0	1	0	0	S4	
0	0	1	0	1	S5	
0	0	1	1	0	S6	
0	0	1	1	1	S7	
0	1	0	0	0	S8	
0	1	0	0	1	S9	
0	1	0	1	0	S10	
0	1	0	1	1	S11	
0	1	1	0	0	S12	
0	1	1	0	1	S13	
0	1	1	1	0	S14	
0	1	1	1	1	S15	
1	X	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't Care

Logic Diagram



CD4514BC- CD4515BC



Appendix 11

Sample and Hold

Datasheet

Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/4435.pdf>

HA-5320



1 μs Precision Sample and Hold Amplifier

November 1996

Features

- Gain, DC 2×10^5 V/V
- Acquisition Time 1.0 μs (0.01%)
- Drop Rate $0.08 \mu\text{s}/V$ (25°C)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- Precision Data Acquisition Systems
- Dielectric to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Description

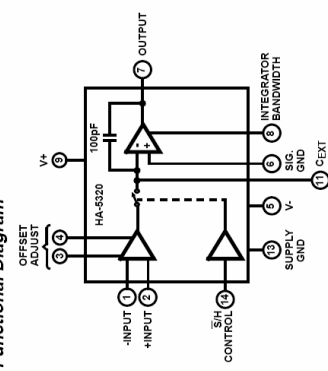
The HA-5320 was designed for use in precision, high speed data acquisition systems. The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCRs. This allows higher speed and latch-free operation. For further information, please see Application Note AN538. For Military grade product refer to the HA-5320/883 data sheet.

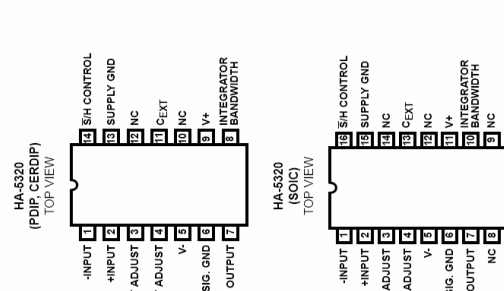
Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
HA1-5320-2	-55 to 25	14 Ld CERDIP	F14.3
HA1-5320-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5320-5	0 to 75	14 Ld PDIP	E14.3
HA8P5320-5	0 to 75	16 Ld SOIC	M16.3
HA8P5320-9	-40 to 85	16 Ld SOIC	M16.3

Functional Diagram



Pinouts



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.
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File Number 2857.3

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Test Circuits and Waveforms

FIGURE 1. CHARGE TRANSFER AND DRIFT CURRENT
(C_H = 100pF)

FIGURE 2. CHARGE TRANSFER TEST

NOTES:

- Observe the "hold step" voltage V_p.
- Compute charge transfer: Q = V_pC_H.
- Observe the voltage "droop", ΔV_O/Δt.
- Measure the slope of the output during hold, ΔV_O/Δt, and compute drift current: I_D = C_H ΔV_O/Δt.

FIGURE 3. DRIFT CURRENT TEST

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

NOTE: Feedthrough in dB = 20log(V_{OUT}/V_{IN}) where:
V_{OUT} = V_{p-p}, Hold Mode,
V_{IN} = V_{p-p}

Application Information

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5320 includes a 100pF MOS hold capacitor sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor, C_{EXT} is used, then a noise bandwidth capacitor of value 0.1C_{EXT} should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor, C_{EXT} should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to 85°C. Teflon® and glass dielectrics offer good performance to 125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

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HA-5320

Typical Application

Figure 5 shows the HA-5320 connected as a unity gain non-inverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor C_{EXT} as shown. As mentioned earlier, 0.1C_{EXT} is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the SH output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer

The small charge capacitance of the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset/pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H (\text{pF}) \times \text{Hold Step Error (V)}$$

$$I_D (\mu\text{A}) = C_H (\text{pF}) \times \frac{\Delta V}{\Delta T} (\text{V/s})$$

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{\text{Hold Capacitance (pF)}}$$

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the SH switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the SH amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time, Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

Typical Performance Curves

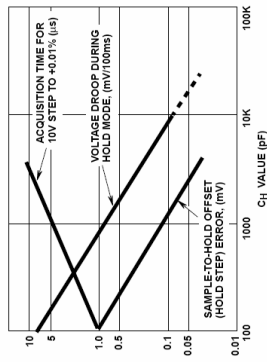


FIGURE 6. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLD CAPACITOR

HA-5320

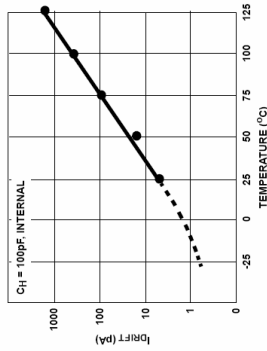


FIGURE 7. DRIFT CURRENT VS TEMPERATURE

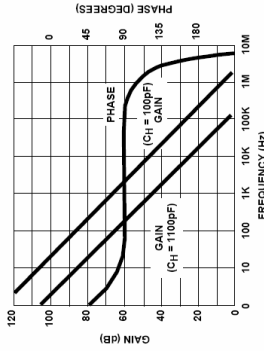


FIGURE 8. OPEN LOOP GAIN AND PHASE RESPONSE

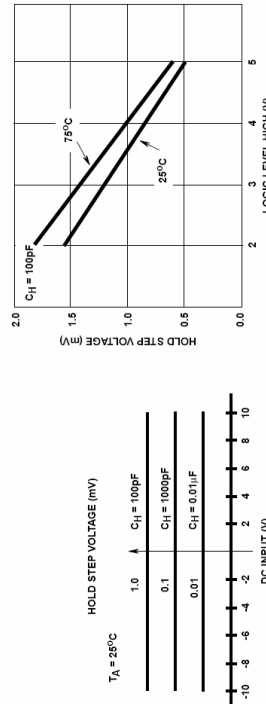


FIGURE 9A. HOLD STEP VS INPUT VOLTAGE

FIGURE 9B. HOLD STEP VS LOGIC (V_{IH}) VOLTAGE

Die Characteristics

5-17

HA-5320

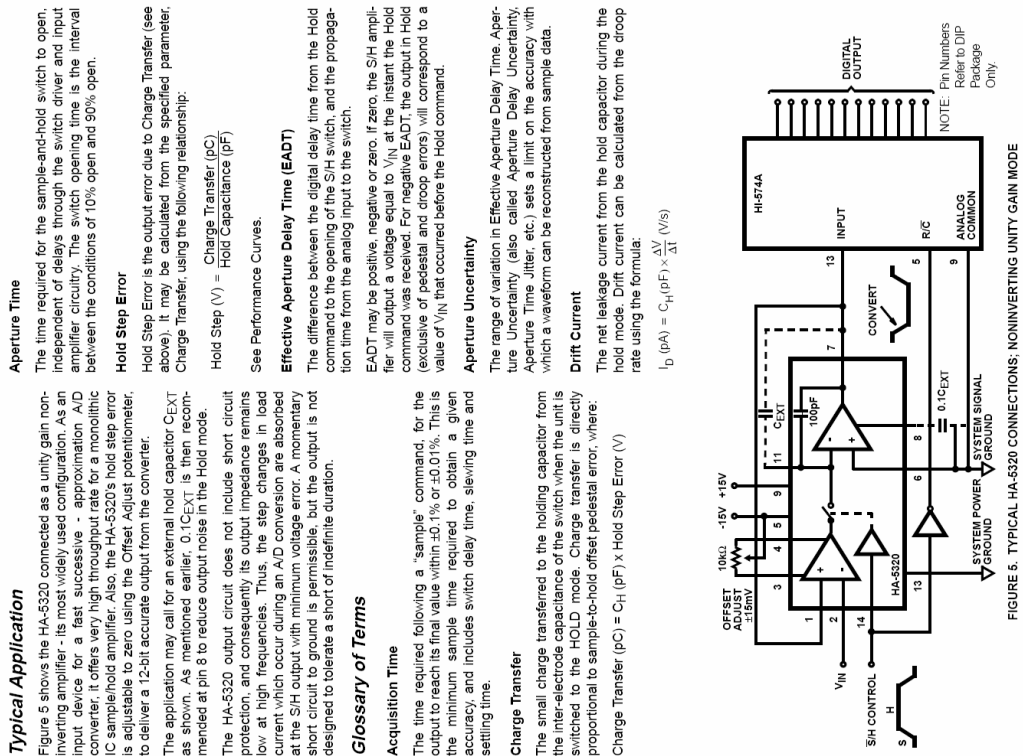


FIGURE 5. TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE

5-16

Appendix 12

RS-422

Datasheet

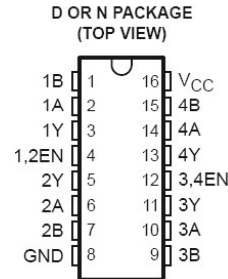
Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/16984.pdf>

MC3486

QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

SLLS097B – JUNE 1980 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11
- 3-State, TTL-Compatible Outputs
- Fast Transition Times
- Operates From Single 5-V Supply
- Designed to Be Interchangeable With Motorola™ MC3486



description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

The MC3486 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \leq 0.2 \text{ V}$	H	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	H	?
$V_{ID} \leq -0.2 \text{ V}$	H	L
Irrelevant	L	Z
Open	H	?

H = high level, L = low level, Z = high impedance (off),
? = indeterminate



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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Appendix 13

Monostable

Datasheet

Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/9595.pdf>

CD4538BC

CD4538BC Dual Precision Monostable

October 1987
Revised January 1999



CD4538BC

Dual Precision Monostable

General Description

The CD4538BC is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active LOW and prevent triggering while active. Precise control of output pulse width has been achieved using internal CMOS techniques. The pulse widths and accuracy are determined by external components R_X and C_X . The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

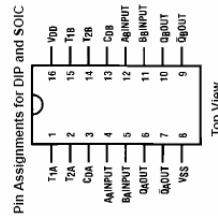
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{CC} (Typ.)
- Low power TTL compatibility: Fan out of 2 driving 74LS or 1 driving 74LS
- New formula: $PW_{OUT} = RC$ (PW in seconds, R in Ohms, C in Farads)
- $\pm 1.0\%$ pulse-width variation from part to part (typ.)
- Wide pulse-width range: 1 μs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current: 5 nA (typ.) @ 5 V_{CC}
- Pin compatible to CD4528BC

Ordering Code:

Order Number	Package Number	Package Description
CD4538BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4538BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
CD4538BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

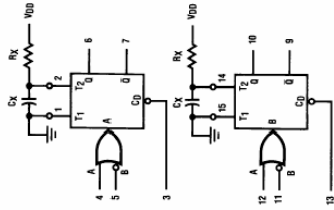


Truth Table

Clear	Inputs		Outputs	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	L	L	H
H	T	H	L	L
H	T	H	L	L

H = HIGH Level
L = LOW Level
T = Transition from LOW-to-HIGH or HIGH-to-LOW
X = One HIGH Level Pulse
L = One HIGH Level Pulse
L = One LOW Level Pulse
X = Irrelevant

Block Diagram



R_X and C_X are External Components
 V_{CC} = Pin 16
 V_{SS} = Pin 8

Logic Diagram

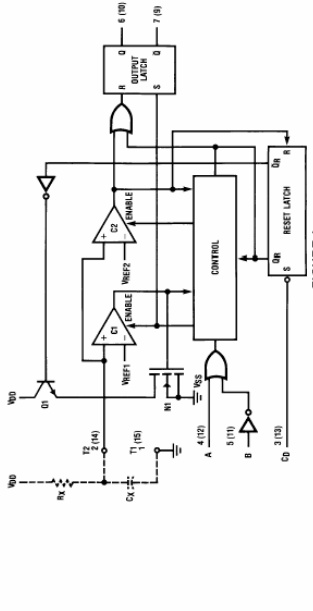


FIGURE 1.

CD4538BC

CD4538BC

Theory of Operation

① POSITIVE EDGE TRIGGER ④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
② NEGATIVE EDGE TRIGGER ⑤ RESET (PULSE SHORTENING)
③ POSITIVE EDGE TRIGGER

Thus, propagation delay from trigger to Q is independent of the value of C_X , R_X , or the duty cycle of the input waveform.

Trigger Operation

The block diagram of the CD4538BC is shown in Figure 1. As shown in Figures 1 and Figure 2, before an input trigger occurs the monostable is in the quiescent state with the output low, and the timing capacitor C_X completely charged to V_{DD} . When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_0 are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1¹. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{AERR} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X , toward V_{DD} . When the voltage across C_X equals V_{AERR} , comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_0 is at $V_{DD}/2$).

It should be noted that in the quiescent state C_X is fully charged to V_{DD} , causing the current through resistor R_X to be zero. Both comparators are 'off' with the total device current due only to reverse junction leakages. An added feature of the CD4538BC is that the output latch is set via the input trigger without regard to the capacitor voltage.

Retrigger Operation

The CD4538BC is retriggered if a valid trigger occurs⁽³⁾ followed by another valid trigger⁽⁴⁾ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{AERR} , but has not yet reached V_{REF2} , will cause an increase in output pulse width T. When a valid retrigger is initiated⁽⁴⁾, the voltage at T2 will again drop to V_{AERR} before progressing along the RC charging curve toward V_{DD} . The Q output will remain high until time T, after the last valid retrigger.

Reset Operation

The CD4538BC may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_0 sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1⁽⁶⁾. When the voltage on the capacitor reaches V_{REF2} , the reset latch will clear and then be ready to accept another pulse. If the C_0 input is held low, any trigger inputs that occur will be inhibited and the Q and \bar{Q} outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_0 input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

FIGURE 3. Retriggerable Monostables Circuitry

FIGURE 4. Non-Retriggerable Monostables Circuitry

FIGURE 5. Connection of Unused Sections

Appendix 14

NAND gate

Datasheet

Note: This Appendix may only contain certain pages of the datasheet, the full datasheet can be found at <http://www.farnell.com/datasheets/21842.pdf>

CD54HC00, CD54HCT00, CD74HC00, CD74HCT00

High Speed CMOS Logic Quad 2-Input NAND Gate



January 1988

Features

- Buffered Inputs
- Typical Propagation Delay: 7ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{HL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, I_i ≤ 1μA at V_{OL}, V_{OH}
- Related Literature
 - CD54HC00F3A and CD54HCT00F3A Military Data Sheet, Document Number 3753

Description

The Harris CD54HC00, CD54HCT00, CD74HC00 and CD74HCT00 logic gates utilize silicon CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally pin compatible with the standard 74LS logic family.

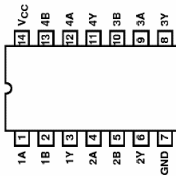
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE NO.	PKG. NO.
CD74HC00E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT00E	-55 to 125	14 Ld PDIP	E14.3
CD74HC00M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT00M	-55 to 125	14 Ld SOIC	M14.15
CD54HC00F	-55 to 125	14 Ld CERDIP	F14.3
CD54HCT00F	-55 to 125	14 Ld CERDIP	F14.3
CD54HC00W	-55 to 125	Water	
CD54HCT00W	-55 to 125	Water	
CD54HC00H	-55 to 125	Die	
CD54HCT00H	-55 to 125	Die	

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

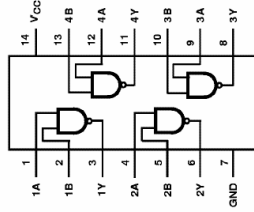
Pinout

CD54HC00, CD54HCT00, CD74HC00, CD74HCT00
(PDIP, CERDIP, SOIC)
TOP VIEW



CD54HC00, CD54HCT00, CD74HC00, CD74HCT00

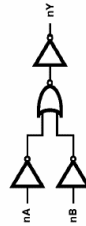
Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
1A	1B	nY
L	L	H
L	H	H
H	L	H
H	H	L

Logic Symbol



Appendix 15

IMU Decoder

Construction

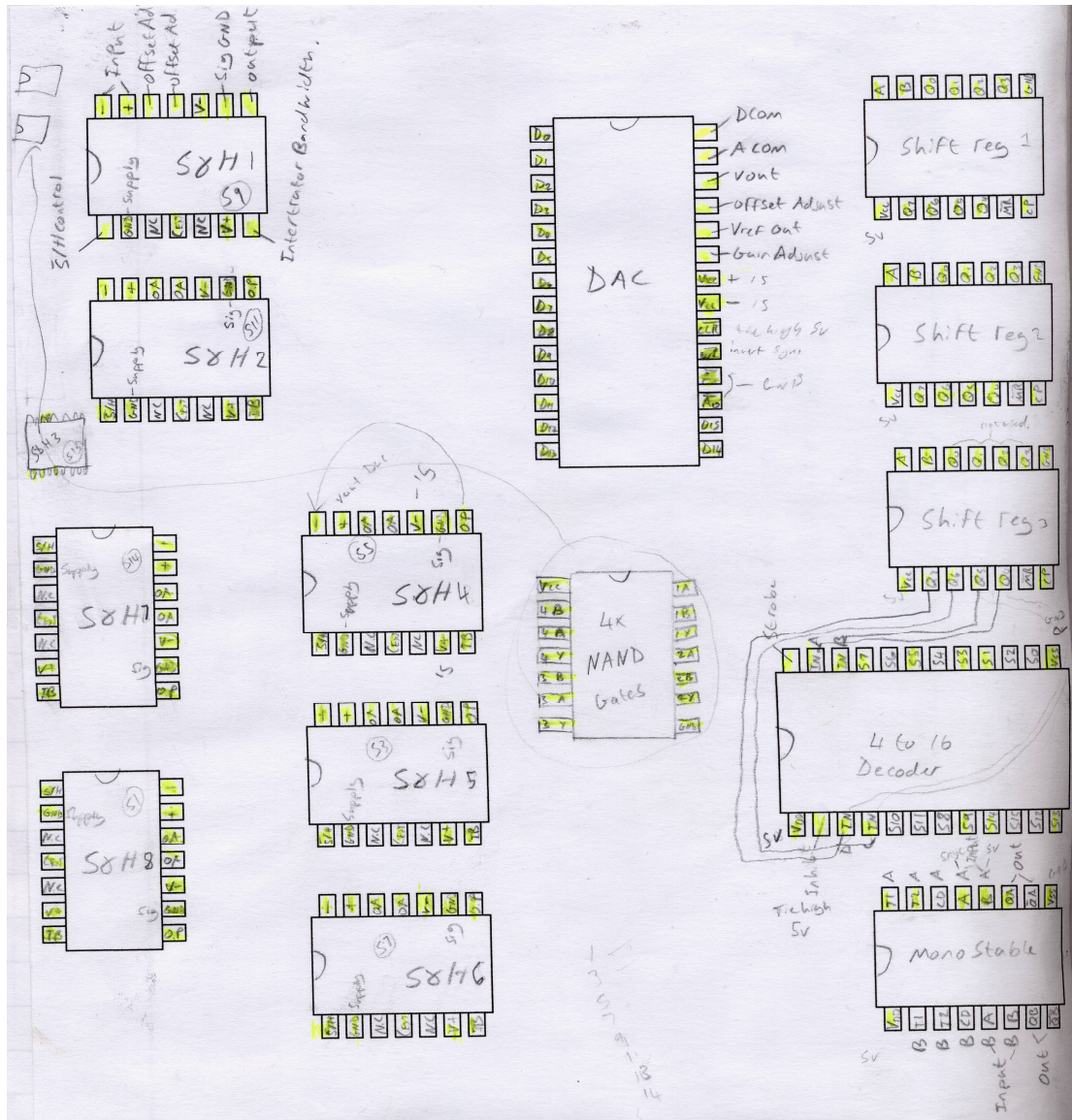


Figure 15.1. Wire Wrapping Wiring Diagram

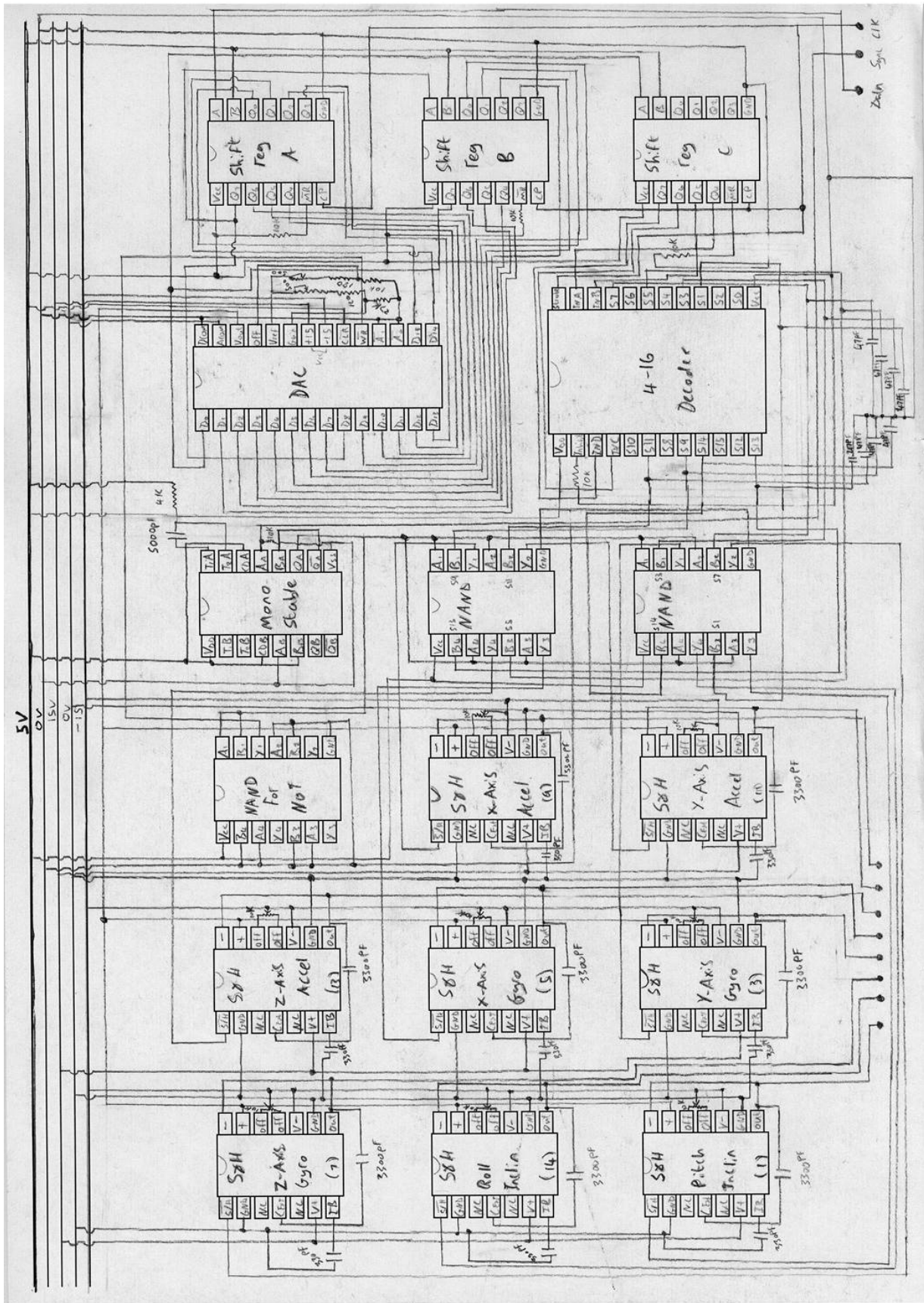


Figure 15.2. Veroboard Wiring Diagram

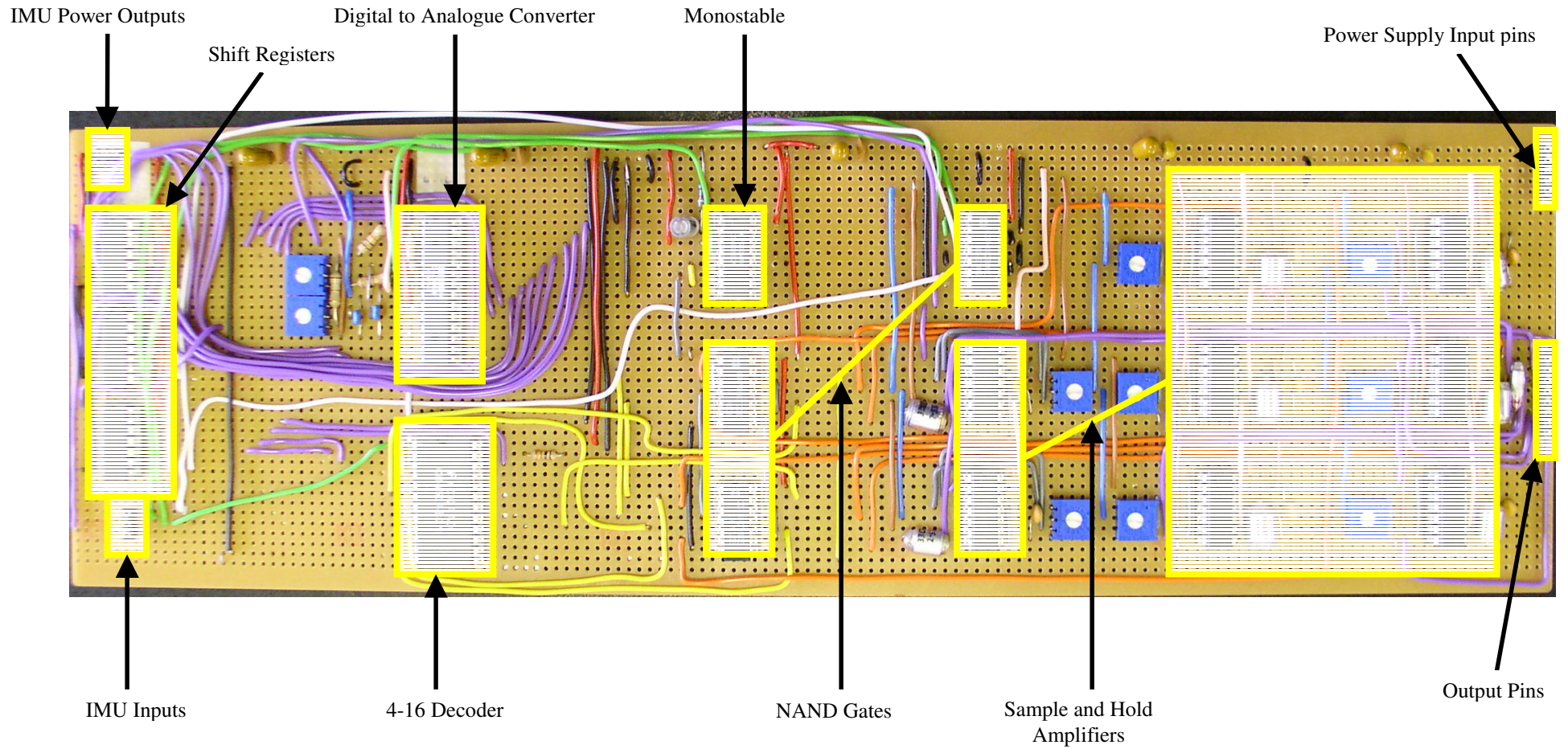


Figure 15.3. Veroboard Decoder Complete

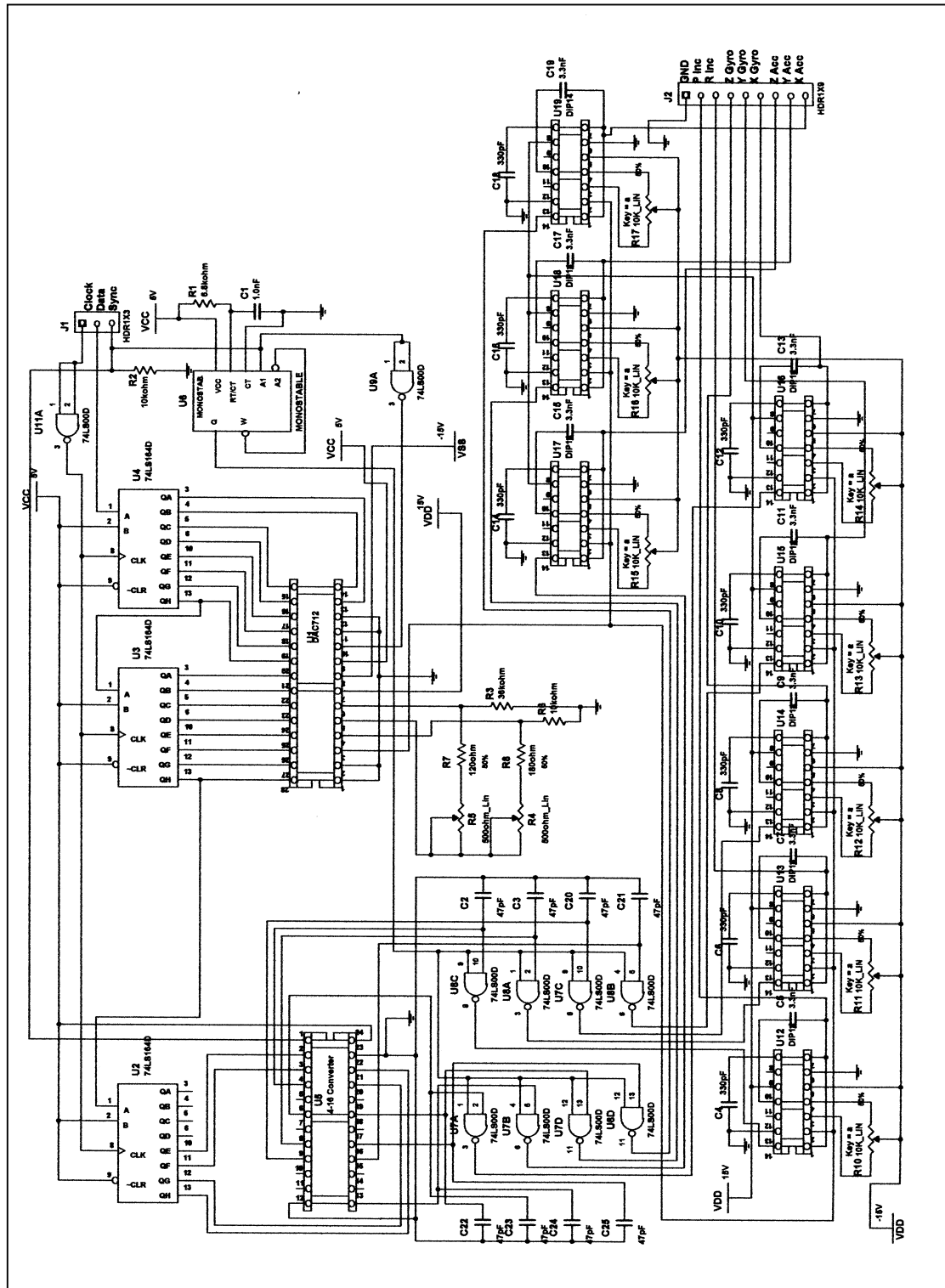


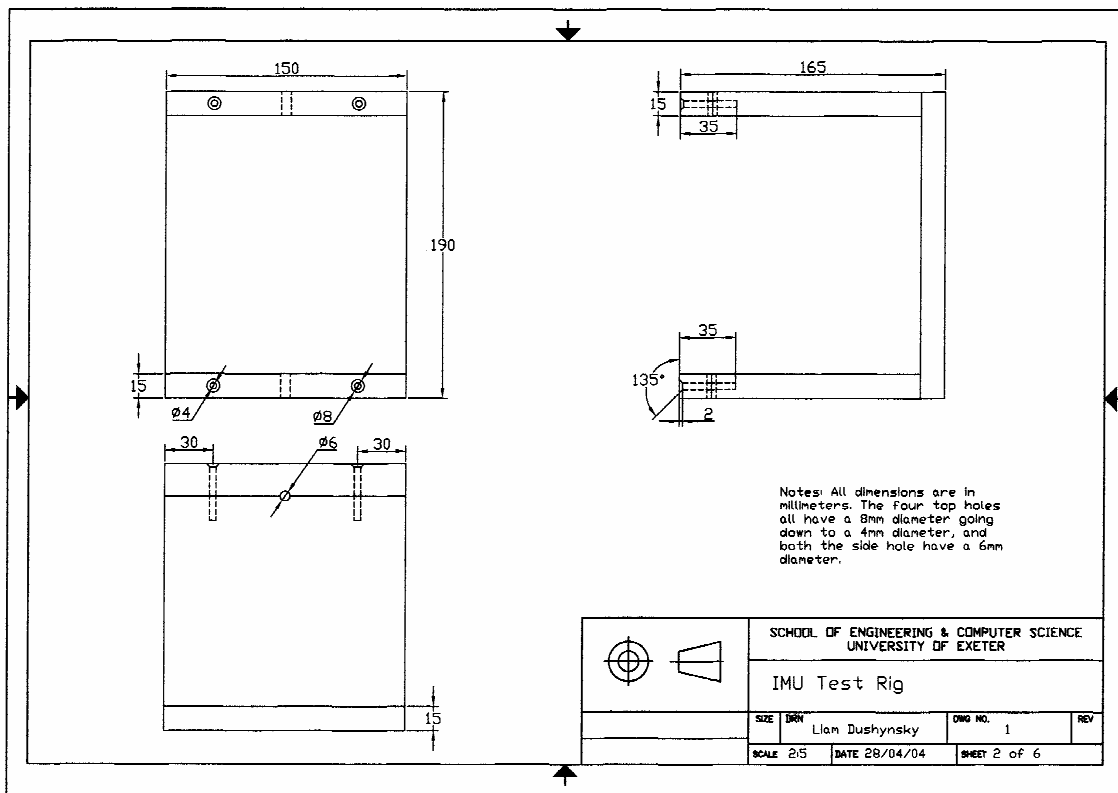
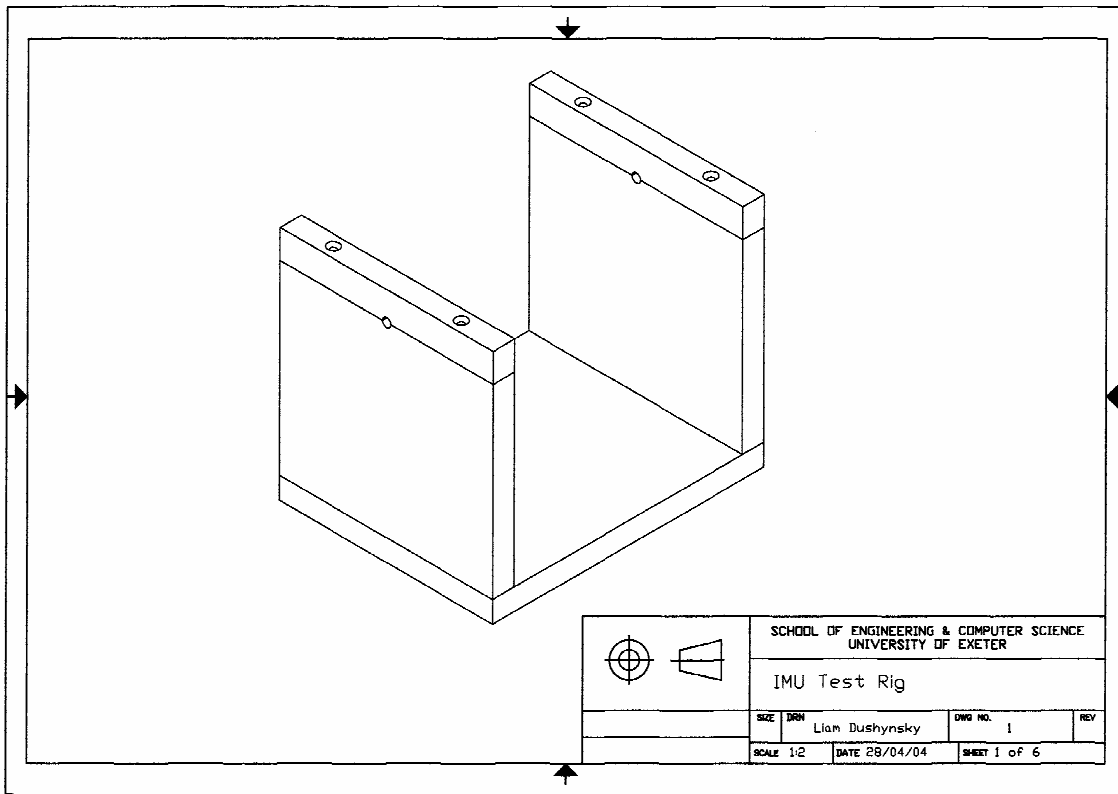
Figure 15.4. Final Decoder Circuit Diagram

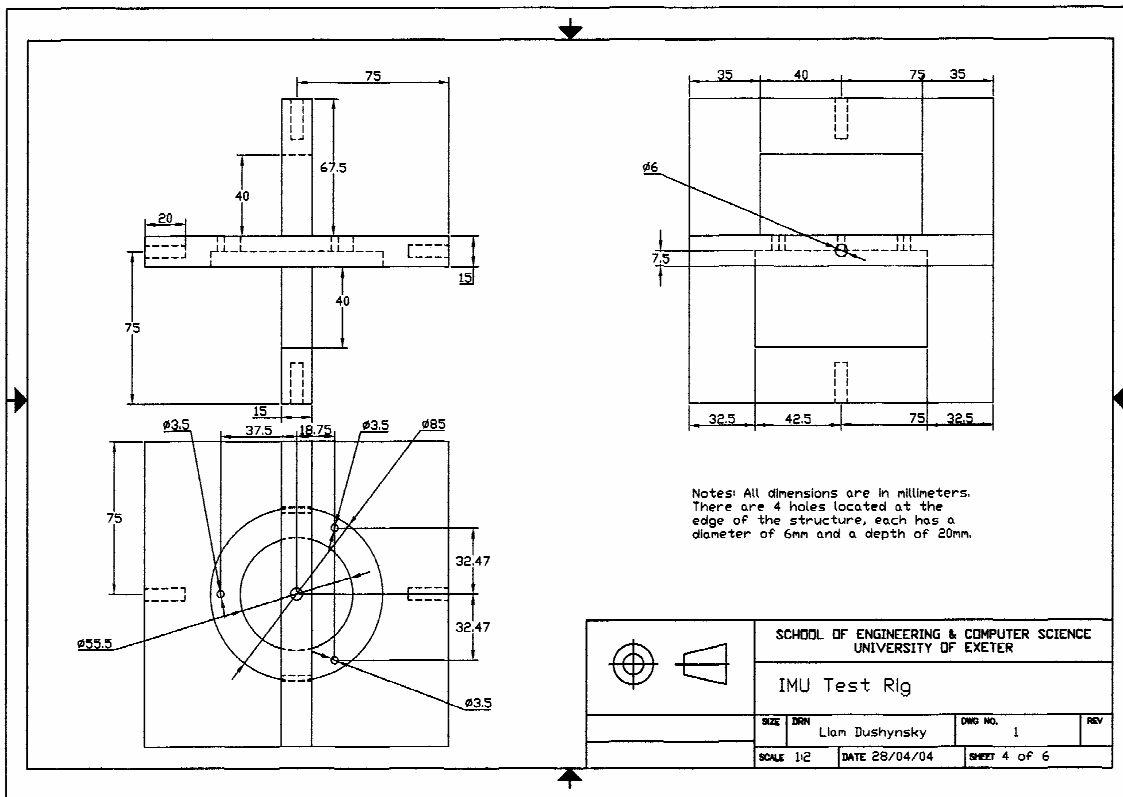
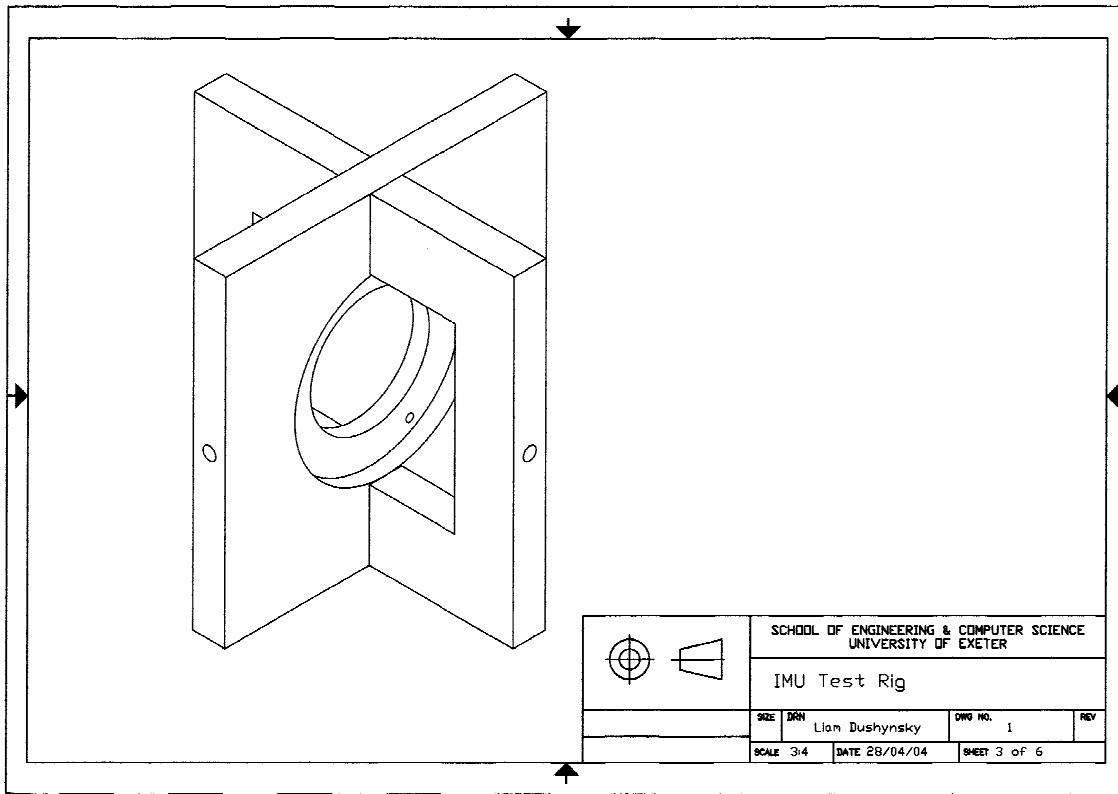
Note: Drafted by A. Tombling Checked by L. Dushynsky

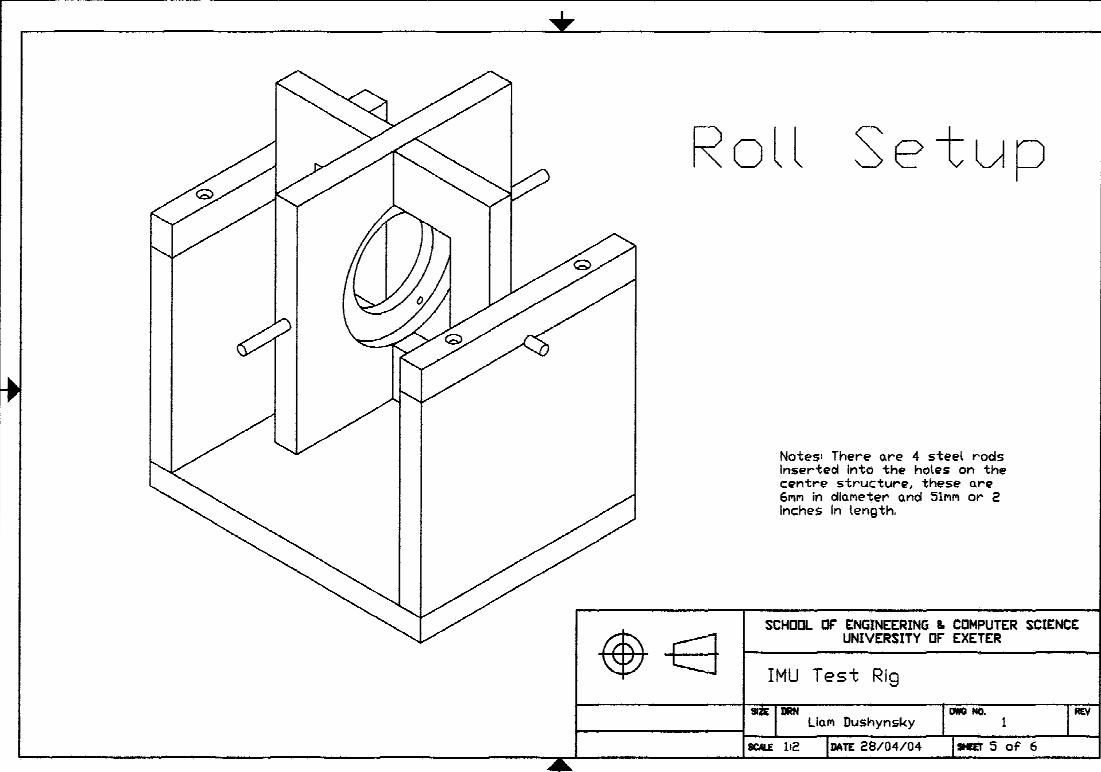
Appendix 16

IMU Test Rig

Construction





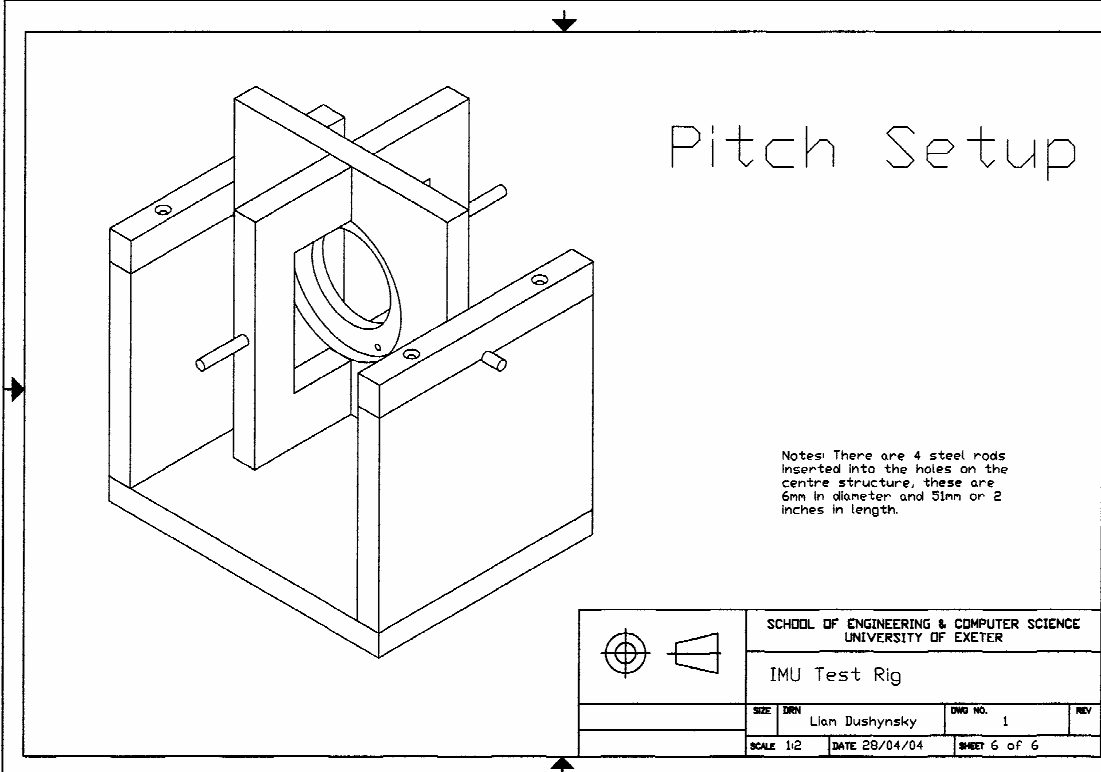




Roll Setup



Notes: There are 4 steel rods inserted into the holes on the centre structure, these are 6mm in diameter and 51mm or 2 inches in length.

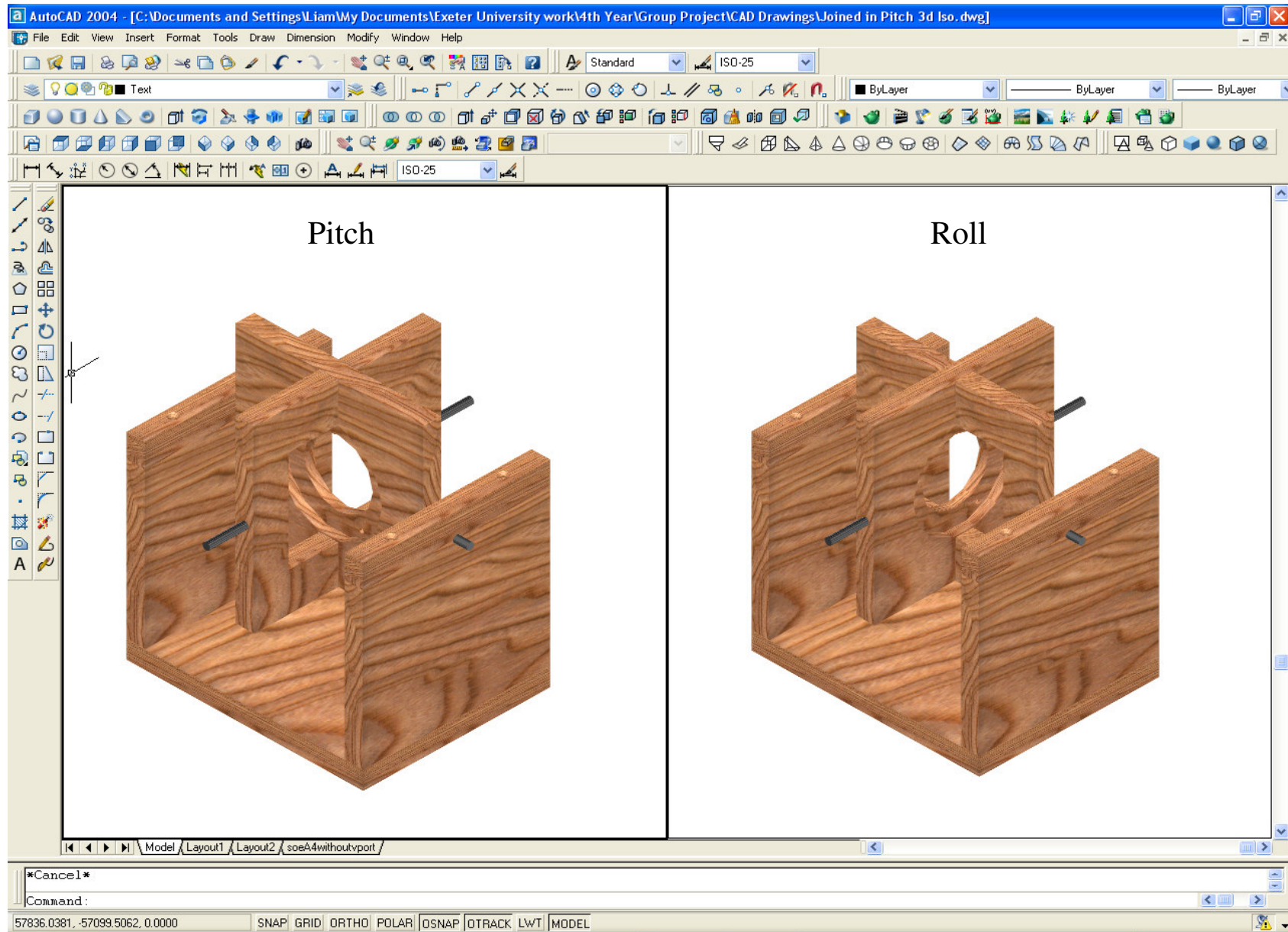
 				SCHOOL OF ENGINEERING & COMPUTER SCIENCE UNIVERSITY OF EXETER			
IMU Test Rig							
SIZE	DRN	Liam Dushynsky	DWG NO.	1	REV		
SCALE	1:2	DATE	28/04/04	SHEET 5 of 6			



Pitch Setup

Notes: There are 4 steel rods inserted into the holes on the centre structure, these are 6mm in diameter and 51mm or 2 inches in length.

 				SCHOOL OF ENGINEERING & COMPUTER SCIENCE UNIVERSITY OF EXETER			
IMU Test Rig							
SIZE	DRN	Liam Dushynsky	DWG NO.	1	REV		
SCALE	1:2	DATE	28/04/04	SHEET 6 of 6			



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