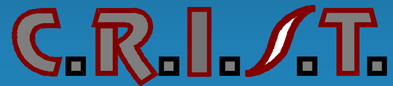


MRAM - present state-of-the-art and future challenges

Dr G. Pan

CRIST
School of Computing, Communication & Electronics
Faculty of Technology,
University of Plymouth,
Plymouth, PL4 8AA, UK

Outline

- **The case for MRAM and its status in 2003/4 and today**
- **Different versions of MRAM**
  - Field writing MRAM – earlier Motorola version
  - Toggled MRAM – 2nd generation Motorola version
  - TAS MRAM – FP5 Strep project NEXT
  - Spin torque MRAM – Best approach to date
  - EMAC MRAM – FP6 Strep project EMAC
- **MRAM research activities at CRIST**
- **Conclusions**

IEEE Distinguished Lecture, 2004 @ Manchester University

Magnetoresistive Random Access Memory: The Path to Competitiveness

Jian-Gang (Jimmy) Zhu
Carnegie Mellon University, Pittsburgh, PA

With the first commercial product on the horizon, magnetoresistive random access memory (MRAM) is on a path to replace static random access memory (SRAM), dynamic random access memory (DRAM), and flash memory (and even disk drives in some applications) as the universal solid-state memory. Non-volatility, fast access time, and compatibility with CMOS technology are three of the most important features that make MRAM potentially superior to other existing memory technologies. To fully exploit these potentials, present MRAM designs need to overcome three major obstacles: stringent fabrication tolerances, relatively high power consumption, and response to write addressing disturbances. Although prototype memory devices have been successfully demonstrated, new, innovative designs are still required to make the technology truly competitive.

In the designs employed by today's MRAM manufacturers, the magnetic moment in a memory element is effectively linear, with its orientation representing the memory state "1" or "0." Switching between the two memory states is done by the Amperean field generated by currents in a pair of orthogonal conducting wires, often referred to as cross-point writing. The cross-point write addressing scheme generates write disturbances because the half-selected memory elements along each of the activated wires experience one of the two field components during a write operation. The result is a stringent requirement for a narrow switching field distribution for all the elements in a memory block, and consequently a stringent fabrication tolerance. The phenomenon is further exacerbated by the possibility of undesired thermally-activated magnetization reversals, especially at small physical dimensions of the memory elements.

- MRAM is on the path to become the universal memory to replace DRAM, SRAM and Flash memory
- MRAM is the enabling technology for computer systems on a single chip

MRAM is the "Holy Grail" of memory

Major industrial players in R&D of MRAM in 2003/4

- NVE
- Freescale Semiconductors Inc. (Motorola)
- Cypress (SMS)
- Agilent
- IBM/INFINEON
- ST/Philips/ Freescale alliance in Crolles
- Altis
- Grandis Inc.
- Renesas Technology
- SONY
- Samsung
- Hitachi
- Toshiba
- …..

Status of industrial players in the end of 2005

- NVE
- Freescale Semiconductors Inc. (Motorola) X
- Cypress(SMS) X
- Agilent
- IBM/INFINEON X
- Altis X
- ST/Philips/ Freescale alliance in Crolles X
- Grandis Inc.
- Renesas Technology

} Joint project on spin MRAM

- SONY - successful demo of 4 kb spin MRAM chip
- Samsung
- Hitachi – achieved low current writing for spin MRAM
- Toshiba
- …..

Spin MRAM is starting to show its commercial potential

Overview of MRAM technology

Selling points of MRAM

- Non-volatile, faster than SRAM. potentially cheap, low power consumption and high integration level.

Competing technologies:

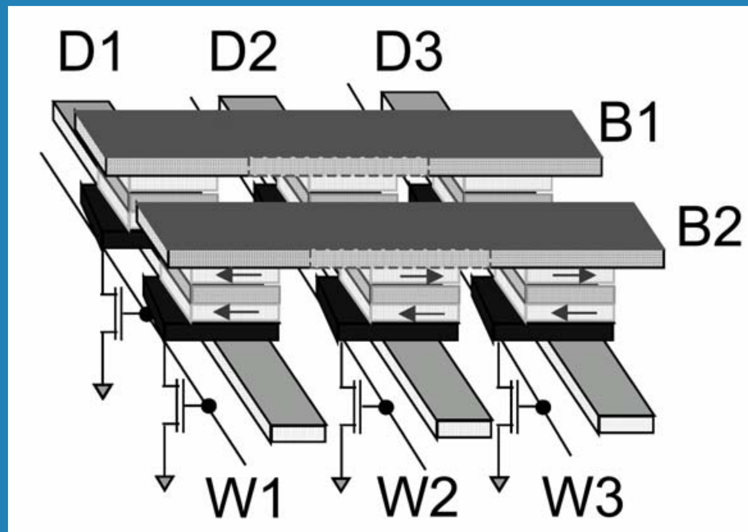
- DRAM, SRAM, Flash memory and other emerging memory technologies such as PCRAM and FeRAM

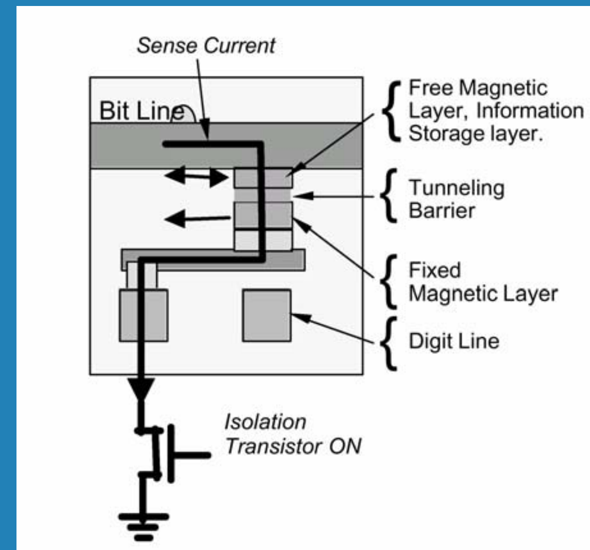
Key performance indicators of various memory technologies

	Non-Volatile		Volatile	
	MRAM (MTJ)	**Flash**	DRAM	SRAM
Bit size	**4-8 F^2**	**2-4 F^2**	**8 F^2**	**100 F^2**
Writing time	**<2 ns**	5– 10 μs	~ 1 ns	~ 1 ns
Access time	**2-40 ns**	40-70 ns	40-70 ns	6-70 ns
Writing voltage	**0.3-5 V**	10-18 V	2.5-5 V	0.8-5 V
Writing Energy	**<100pJ**	~ 300 pJ	10-200 pJ	<200pJ
Radiation hardness	**excellent**	poor	poor	poor

Field writing MRAM – Motorola Version 1

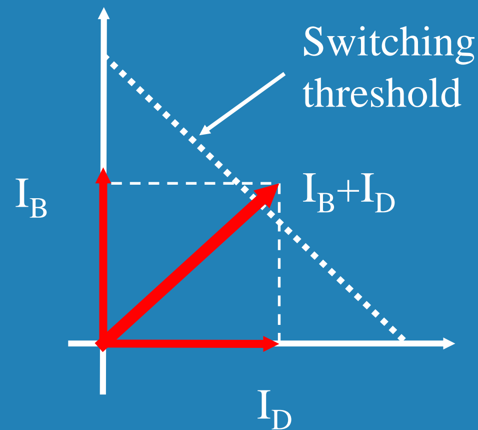
One transistor per cell structure

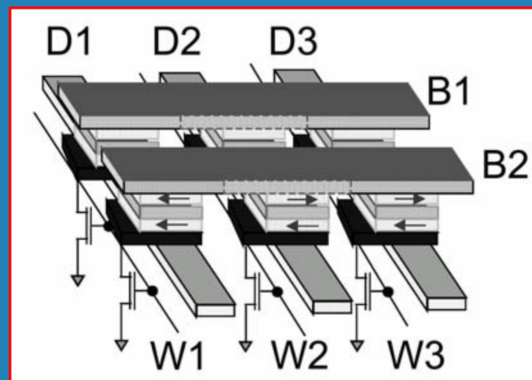


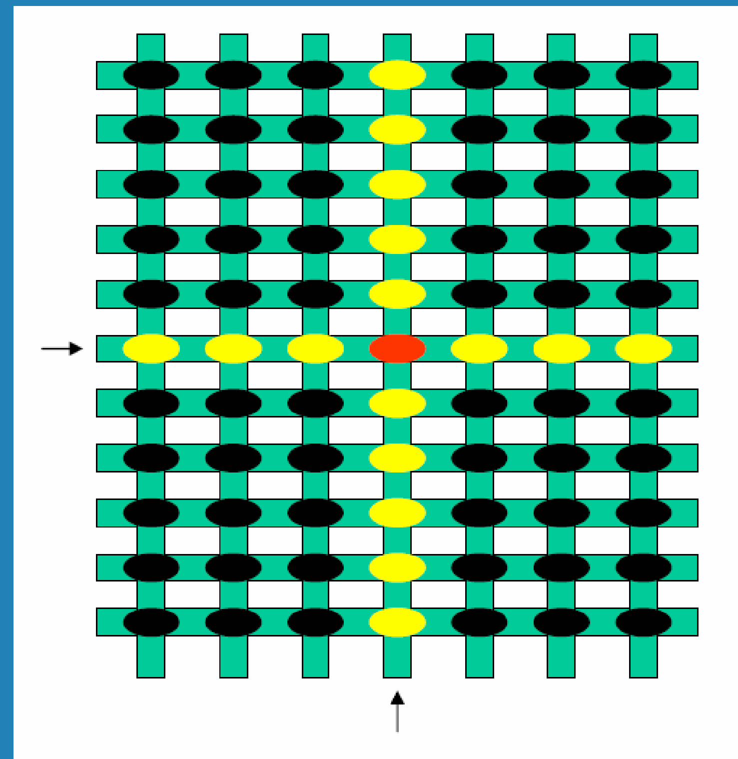


Writing – 2D magnetic selection

- is accomplished by I_B+I_D . Each line is ½ selected and provides half of the field required to switch the free layer of a cell.







Major features:

- Non-volatile.
- One transistor per cell architecture.

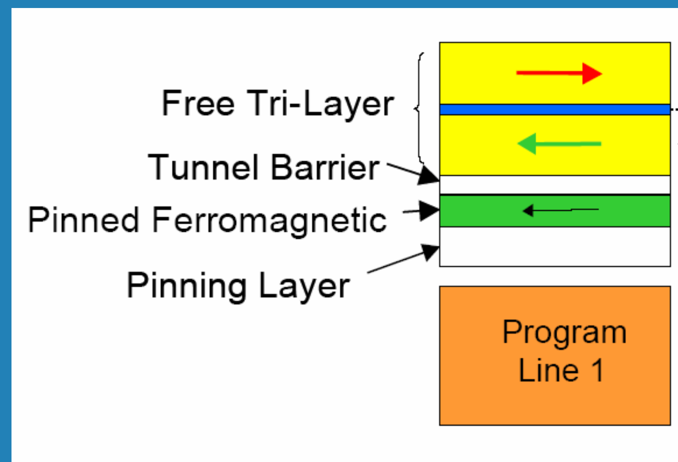
Major limitations of FW MRAM:

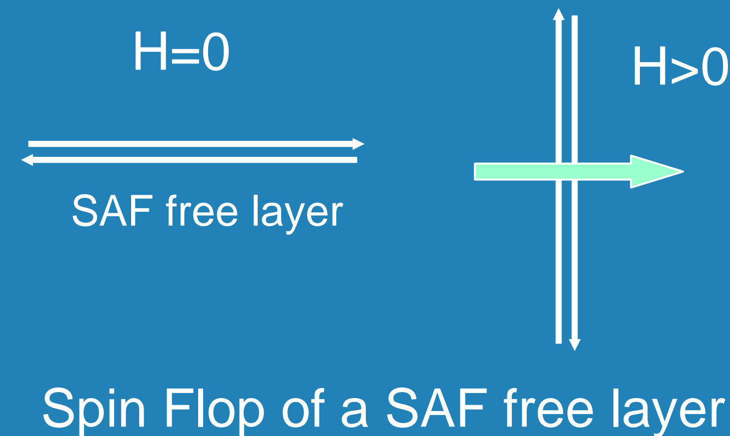
Because writing is i-field based (2D magnetic selection), it has the following limitations:

- 1/2 selected lines could cause addressing errors due to switching field distribution of the cells.
- FW limits the level of integration, difficult to implement at high density due to stray field cross interference.
- No parallel writing at high density due to cross interferences.
- High power consumption due to inductive writing, increasing with reduction of cell sizes, typical writing current more than 10 mA.

Toggled MRAM – Motorola version 2

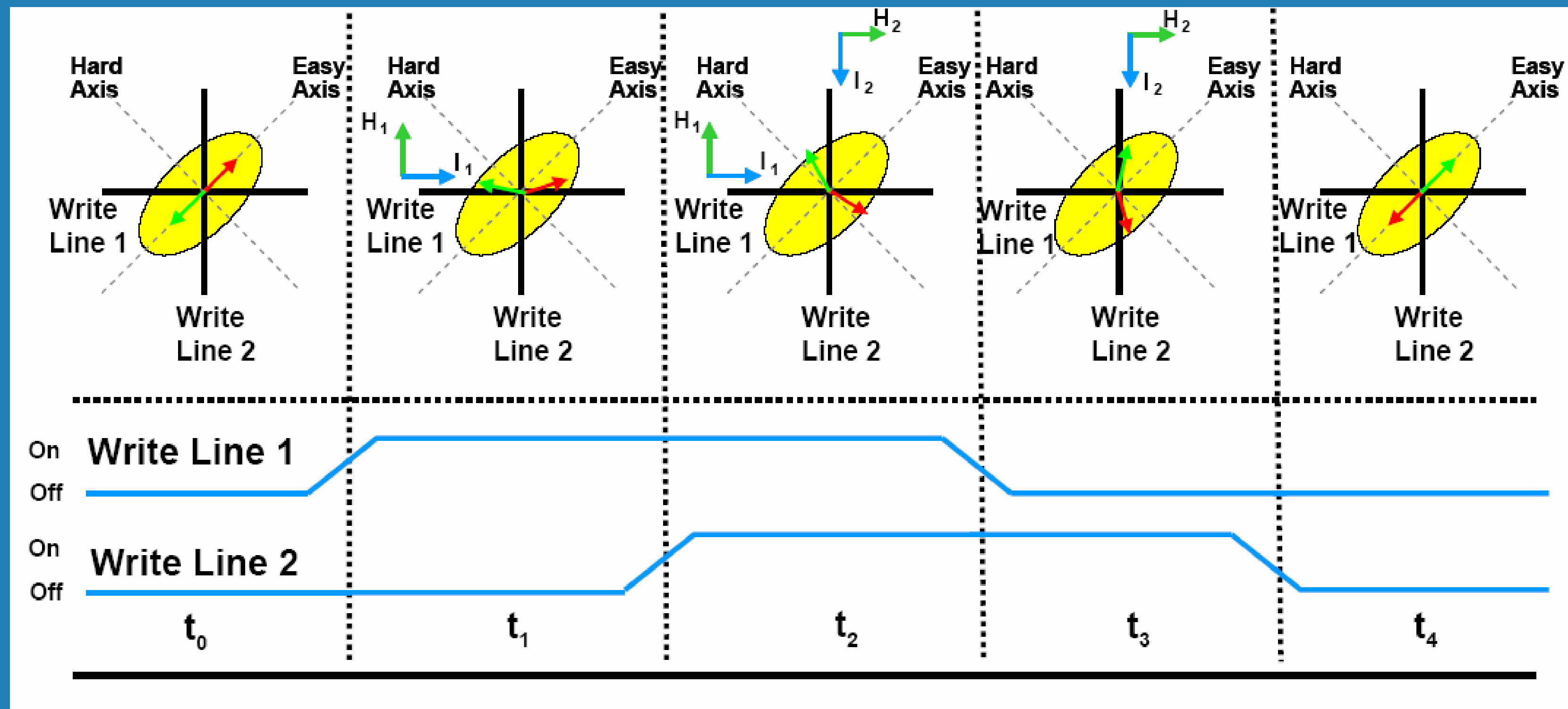
- Proposed at Motorola by the late Leonid Savtchenko: US Patent 6,549,906
- Write operation is a rotation of a balanced SAF
- Toggle rather than “forced” write





Spin Flop of a SAF free layer

♌ Toggled MRAM switching sequence

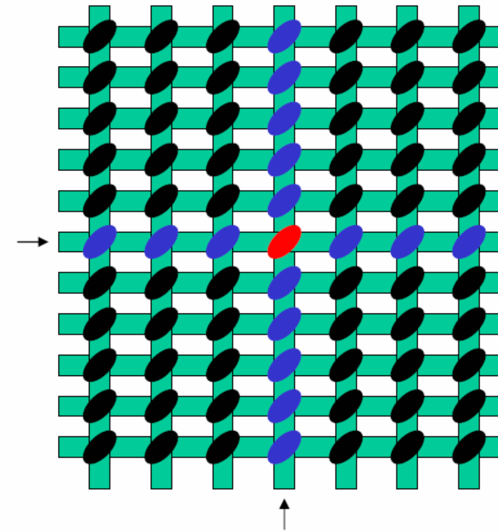


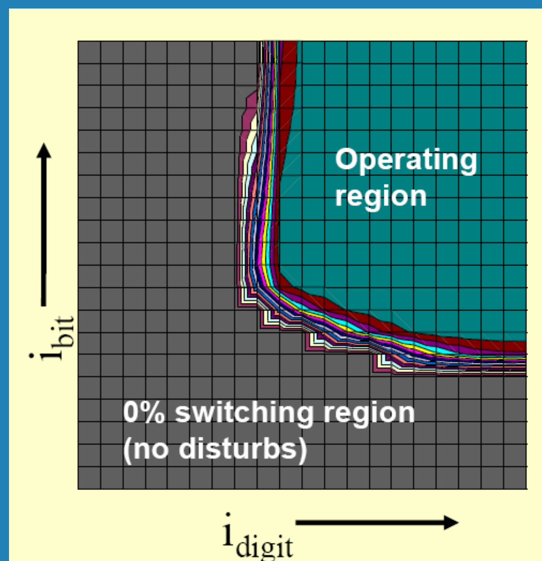
A 4Mb MRAM integrated into a 0.18μm CMOS process has been successfully demonstrated in 2004

- Toggle writing scheme
- 25 ns read and write cycle times

Advantages of toggled MRAM

- High bit disturb margin
- All bits along ½-selected current lines have ***increased*** energy barrier during programming
- Requires overlapping pulse sequence for switching

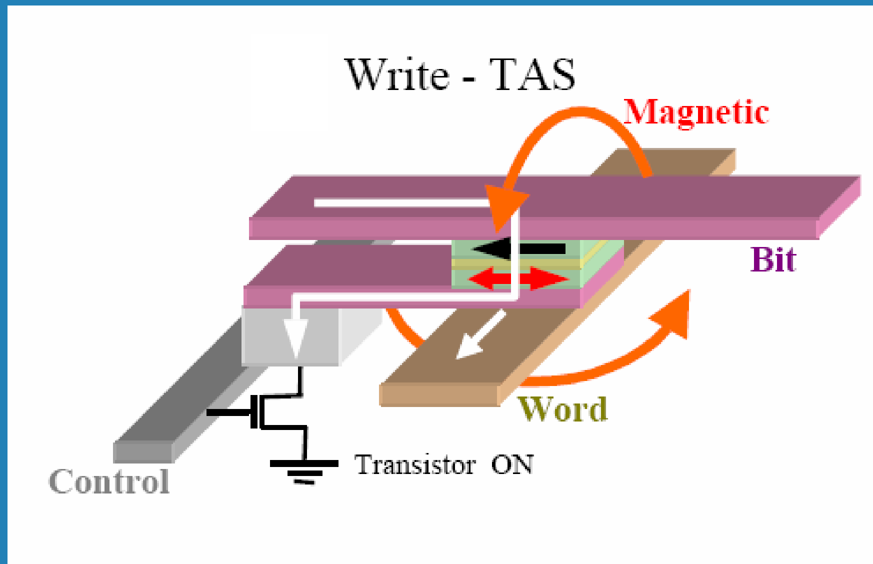


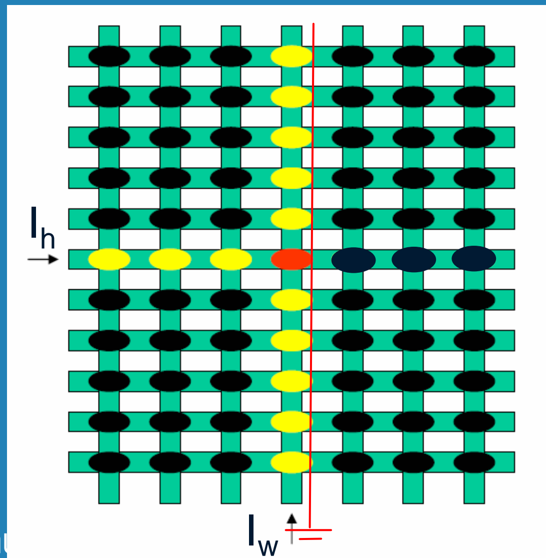


limitations of toggled MRAM

How to achieve small writing current is still an issue, particularly at small cell sizes

Thermally assisted MRAM (TAS MRAM)





Advantages:

- Semi-1D magnetic selection
- Less likely to have addressing errors by ½ -selection as in FW MRAM due to smaller writing current at high temperature.
- Less power consumption.

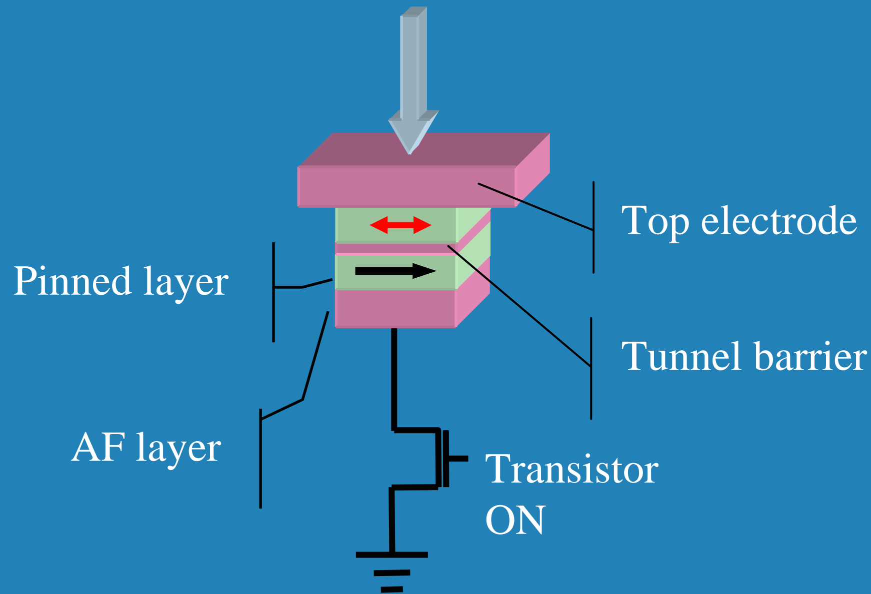
Drawbacks:

One more wire than FW for writing.

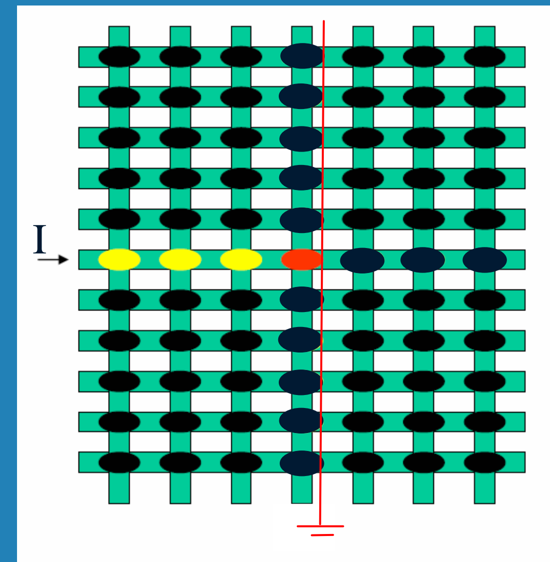
Challenges:

How to achieving high heating efficiency and low heating current.

Spin torque MRAM



Basic principle:
If a highly spin polarised current flows into a ferromagnetic layer, there is a 'torque' applied by the injected electron spins on the local moment that tends to induce a precession of the local magnetisation along this spin direction.



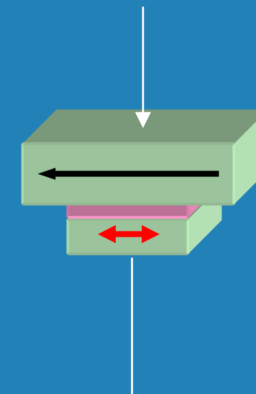
1-D magnetic selection, spin torque writing with much less current.

Spin polarised current induced magnetic switching

Precession Spin transfer Damping

$$\frac{d\mathbf{M}}{dt} = -\gamma \mathbf{M} \times \mathbf{H}_{eff} + \frac{\gamma a_J}{M_s}\mathbf{M} \times (\mathbf{M} \times \hat{\mathbf{M}}_p) + \frac{\alpha}{M_s}\mathbf{M} \times \frac{d\mathbf{M}}{dt},$$

This phenomenon was predicted by Slonczeski* and Berger** respectively in 1996, and subsequently proved experimentally by various researchers since 2000.

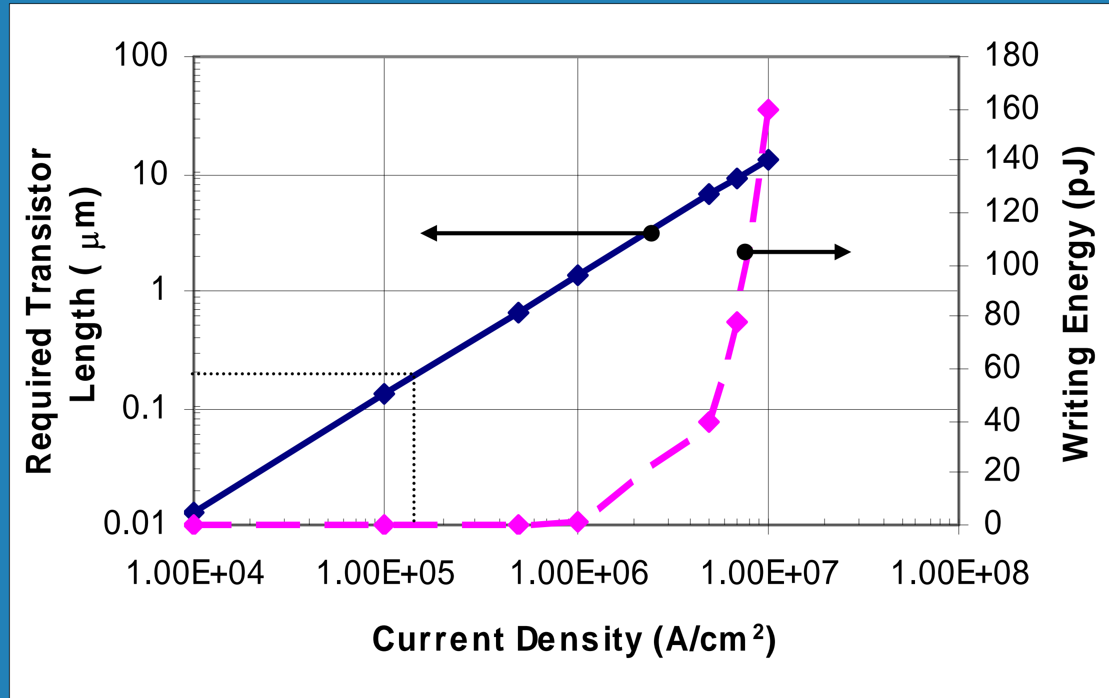


*J. C. Slonczewski, J. Magn. Magn. Mater. **159**, L1 (1996). US patent 5,695,864,
** L. Berger, Phys. Rev. B **54**, 9353 (1996).

Advantages of spin torque writing

- **Retaining all the good features of** the previous versions of MRAM
- **No addressing errors**: The writing process uses a much smaller current that is only flowing through the addressed cell.
- **Multi-bit (parallel) writing**: As it has no half selection issue, it will not affect adjacent cells, fully compatible with parallel writing, whatever the integration level.
- **Low power consumption**: The write current being significantly reduced, the power consumption of writing and reading operation is minimised.
- **Potentially high integration level:** if writing current can be significantly reduced.

Key parameters– Junction RA and critical current density for switching, J_c



The scalability of spin MRAM is determined by the required transistor length due to saturation current of CMOS transistors. Jc needs to be reduced at least down to 1MA/cm² for achieving a competitive bit density.

Typical parameter values

- If critical current density for switching is 10MA/cm^2).
- For a junction size of 0.2x0.2 =0.04 μm^2, the required minimum writing current is 4 mA.
- The maximum allowed writing current is constrained by the junction breakdown voltage,

$$V < 0.8\ V_B.$$

$$J < 0.8\ V_B/RA.$$

- For V_B= 0.5 V, RA < 4 Ω-μm^2.
- If RA is 3 Ω-μm^2, J>133 mA/μm^2. The CIMS writing current is 5 mA for cell size of 0.04 μm^2, which requires the CMOS to allow such a current to go through as well. For CMOS with I_{sat} of 500 μA/μm, the CMOS length will be 10 μm.
- J_c needs to be reduced at least by one order of magnitude.

Technical challenges for spin torque MRAM

- The reduction of the critical current density. At least 1MA/cm^2. Lower J_c means higher integration level and lower power consumption.

- MTJs with low RA, high MR and V_b, for improved process tolerance, which will make the MRAM technology more competitive than its rivals.

The discovery of MgO MTJ

- MgO MTJ with 1000% MR was theoretically predicted by Mathon et al & Butler et al in 2001 and experimentally realised by IBM and Anelva in 2002 and 2004, respectively.
- Crystalline tunnelling barrier produces much higher MR ratio for better signal amplitude and reliability, 230% in 2004 and 355% in 2005.
- Higher spin polarisation in writing current for reduced critical current density for switching.
- Thicker barrier layer for better process tolerance.

PHYSICAL REVIEW B, VOLUME 63, 220403(R)

Theory of tunneling magnetoresistance of an epitaxial Fe/MgO/Fe(001) junction

J. Mathon and A. Umerski
Department of Mathematics, City University, London EC1V 0HB, United Kingdom
(Received 21 December 2000; published 10 May 2001)

PHYSICAL REVIEW B, VOLUME 63, 054416

Spin-dependent tunneling conductance of Fe|MgO|Fe sandwiches

W. H. Butler, X.-G. Zhang, and T. C. Schulthess
Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831-6114

J. M. MacLaren
Department of Physics, Tulane University, New Orleans, Louisiana 70018
(Received 21 June 2000; published 8 January 2001)

LETTERS

Giant tunnelling magnetoresistance at room temperature with MgO (100) tunnel barriers

STUART S. P. PARKIN[1]*, CHRISTIAN KAISER[1], ALEX PANCHULA[1], PHILIP M. RICE[1], BRIAN HUGHES[2], MAHESH SAMANT[1] AND SEE-HUN YANG[1]
[1]IBM Research Division, [2]Infineon Technologies, IBM Almaden Research Center, IBM-Infineon MRAM Development Alliance, 650 Harry Road, San Jose, California 95120, USA
*e-mail: parkin@almaden.ibm.com

APPLIED PHYSICS LETTERS **86**, 092502 (2005)

230% room-temperature magnetoresistance in CoFeB/MgO/CoFeB magnetic tunnel junctions

David D. Djayaprawira,[a)] Koji Tsunekawa, Motonobu Nagai, Hiroki Maehara, Shinji Yamagata, and Naoki Watanabe
Electron Device Equipment Division, Anelva Corporation, 5-8-1, Yotsuya, Fuchu-shi, Tokyo 183-8508, Japan

Shinji Yuasa,[b)] Yoshishige Suzuki,[c)] and Koji Ando
Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki 305-8568, Japan

Low switching current achieved by Grandis Inc. and Singulus Technologies

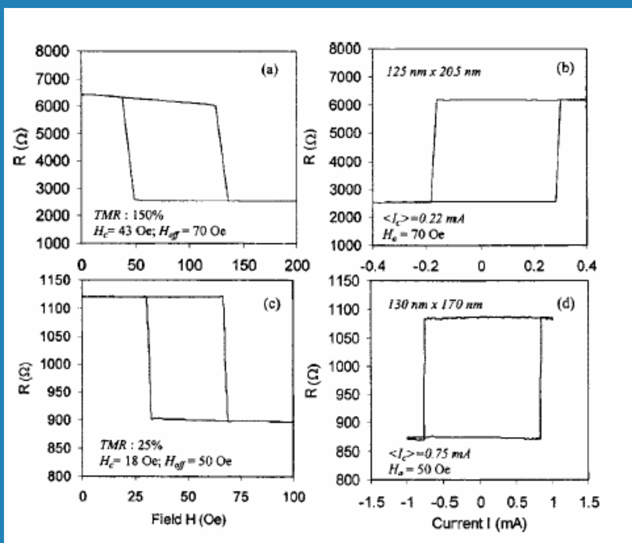
Spin transfer switching and spin polarization in magnetic tunnel junctions with MgO and AlO_x barriers

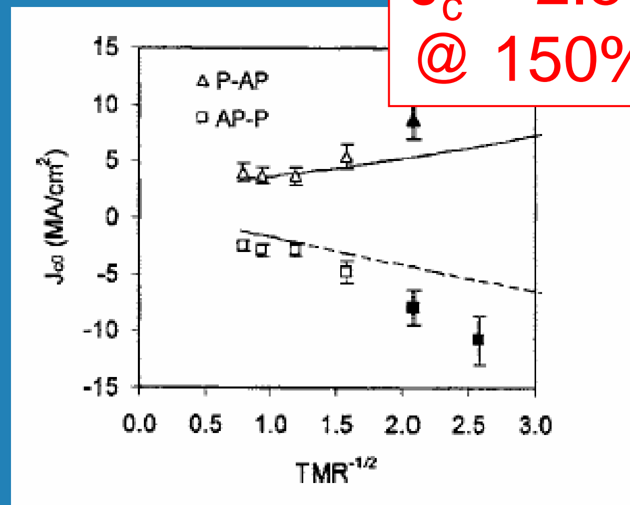
Zhitao Diao, Dmytro Apalkov, Mahendra Pakala, Yunfei Ding,
Alex Panchula, and Yiming Huai[a)]
Grandis Inc., 1123 Cadillac Court, Milpitas, California 95035

(Received 21 July 2005; accepted 7 October 2005; published online 1 December 2005)

We present spin transfer switching results for MgO based magnetic tunneling junctions (MTJs) with large tunneling magnetoresistance (TMR) ratio of up to 150% and low intrinsic switching current density of $2-3\times10^6$ A/cm^2. The switching data are compared to those obtained on similar MTJ nanostructures with AlO_x barrier. It is observed that the switching current density for MgO based MTJs is 3 to 4 times smaller than that for AlO_x based MTJs, and that can be attributed to higher tunneling spin polarization (TSP) in MgO based MTJs. In addition, we report a qualitative study of TSP for a set of samples, ranging from 0.22 for AlO_x to 0.46 for MgO based MTJs, and that shows the TSP (at finite bias) responsible for the current-driven magnetization switching is suppressed as compared to zero-bias tunneling spin polarization determined from TMR. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2139849]

J_c = 2.5 MA/cm^2
@ 150% MR





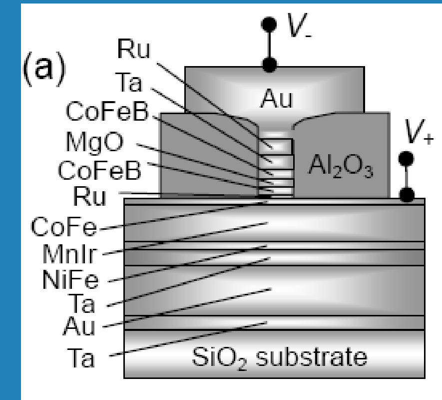
Low switching current density achieved by Hitachi on MgO

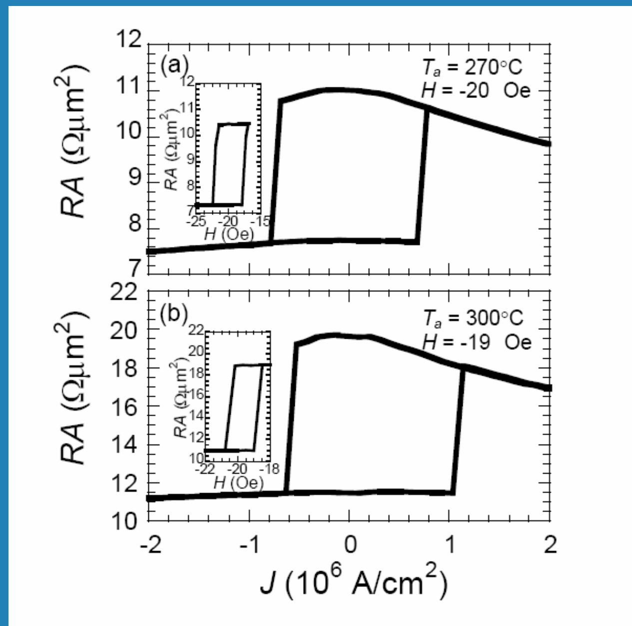
Current-driven magnetization switching in CoFeB/MgO/CoFeB magnetic tunnel junctions

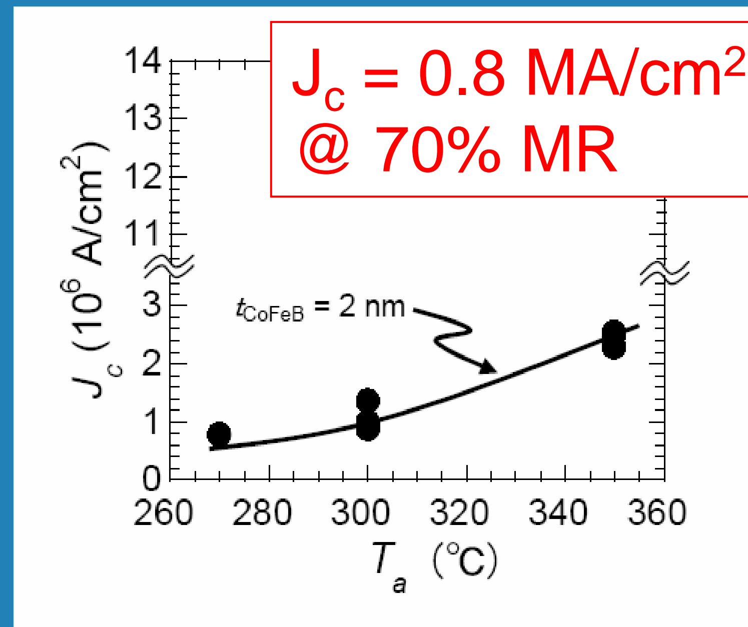
Jun HAYAKAWA[1,2], Shoji IKEDA[2], Young Min LEE[2], Ryutaro SASAKI[2], Toshiyasu MEGURO[2], Fumihiro MATSUKURA[2], Hiromasa TAKAHASHI[1,2], and Hideo OHNO[2]

1. Hitachi, Ltd., Advanced Research Laboratory, 1-280 Higashi-koigakubo, Kokubunji-shi, Tokyo 185-8601, Japan

2. Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan







C.R.I.S.T.

SONY demonstrated 4 kb memory cell for MgO spin torque MRAM on 180 nm CMOS process in Dec 2005

Less power, more scaling
In spin-torque-transfer MRAM, data is written by flowing spin-polarized electrons through the tunneling magnetoresistance element to change the magnetized orientation of the free layer. Since it does not employ an external magnetic field, spin-torque MRAM consumes less power and is more scalable than conventional MRAM. Its construction is identical to that of conventional MRAM in other respects.

Sony researchers built a 4-kbit memory cell in a 180-nanometer CMOS process with four-level metal, according to the paper the company present in Washington at IEDM. The MTJ was built of optimized CoFeB material. Sony has also used CoFeB for conventional-MRAM development.

The researchers verified data write speeds of 2 nanoseconds for the experimental device. Circuit simulations indicate the same speed for reads. The current required to switch the free layer's orientation was 200 microamps, or 1/30 the power required for a conventional MRAM.

Write speed: 2 ns
Writing current: 0.2 mA
Writing power: 1/30 of FW MRAM

Grandis and Renesas joint project

Renesas, Grandis to Collaborate on Development of 65 nm MRAM Employing Spin Torque Transfer

Renesas Technology and Grandis, Inc. have agreed to collaborate on the development of 65 nm process MRAM (Magnetic Random Access Memory) employing spin torque transfer writing technology. Renesas Technology will start to ship microcomputers and SoC products incorporating 65 nm process STT-RAMTM in the near future.

MRAM uses magnets as memory cells. It is a type of random access memory that stores data based on the magnetic orientation of the magnets. MRAM is non-volatile memory that enables data to be retained when power is cut off while also providing high-speed operation and unlimited rewriting capability. This ability to implement functions provided by various kinds of memory has led to high expectations of MRAM as next-generation memory. Most of the MRAM presently under development is based on conventional magnetic field data writing, which supports fast operation speeds. However, in future more ultra-fine processes, MRAM would require very large writing currents. This has caused attention to focus on spin torque transfer writing technology for MRAM using a 65 nm or finer process.

Spin-Injection MRAM

Europe launches a consortium to develop a scalable 1-Mask MRAM

Technology will run on a commercial CMOS production line and be used as embedded memory for products such as sensors and ID tags.

> Budget : 4.2 M€ with EC contribution of 2.2 M€
> Objective: Develop advanced CMOS devices using front-end embedded magnetic materials
> Partners: CNRS (FR), CEA (FR), FRAUNHOFER-IMS (GE), ARC (AU), UNIVERSITY OXFORD (UK), SPINTRON (FR), SEMITOOL (UK), UJF (FR), TOPLINK INNOVATION (FR)

The European Commission announced today the official launch of a Sixth Framework Programme (FP6) Specific Targeted Research aimed at developing advanced CMOS devices using front-end embedded magnetic materials. This technology will be applied to 65nm-scalable 1-Mask Magnetic Random Access Memories (MRAM).

The MRAM idea is based on spin injection through tunnelling barrier, aiming to realise a device based on FM/MgO/Si following the RT spin injection in FM/MgO/GaAs.

MRAM research activities at CRIST

- DTI MNT project – 300mm BIBD MRAM deposition tool, £1.65M in grant value, started in Oct 2005.
- Our roles: Film deposition, microfabrication and characterisation of MTJ films & devices.
- Facilities we have:
  - Industrial standard cleanroom (class 10, 100 and 1000)
  - Sputter-deposition, microfabrication (0.8 μm minimum feature size),
  - Fully computer controlled magneto-transport and spin torque measurement instruments using Labview and Keithley source/measurement meters.
  - High sensitivity VSM
  - Magnetic field annealing system for two inch wafers and up to 5000 Oe.
  - LLG spin torque simulation software
  - Electron microscopes
  - Nordiko 9550 GMR deposition tool – cassette for sixteen 4-inch wafers, 6-targets, load-locked, semi-UHV.

Nordiko 9550 GMR tool

Conclusions

- The case for MRAM as a universal memory is still valid.
- The discovery of MgO MTJ has brought new life to MRAM.
- Spin torque MRAM is so far the best known MRAM idea and significant progresses have been made in the past year.
- New materials research, spin engineering and innovations are required to further increase the MR and reduce the Jc in order for MRAM to compete with other memory technologies.
- The search for better MRAM ideas won't stop at spin MRAM. Better ideas may be developed as scientific breakthroughs being achieved in spintronics field.