




PCM memories: an overview

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Outline

- PCM concept and basic operation
- Modeling
 - ▶ Switching
 - ▶ Set/Reset programming
- Cell structures and scaling perspectives
- Reliability issues
 - ▶ Retention, Drift
- Conclusions



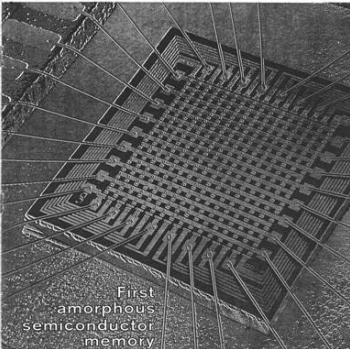
Phase Change Memory

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Amorphous semiconductors: jury still out 56
 Designing low-noise bipolar amplifiers 82
 The big gamble in home video recorders 89

A MICROELECTRONICS PUBLICATION
September 28, 1971

Electronics



First amorphous semiconductor memory


1970
Die: 122 mil X 131 mil
Capacity: 256 bits
Reset: <200 mA, < 25V, 5 ms
Set: 5 mA, ~ 25V, 10 ms
Read: 2.5 mA, < 5V

“Nonvolatile and Reprogrammable, the Read-Mostly Memory is Here,” R. G. Neale, D. L. Nelson, and Gordon E. Moore, *Electronics* (Sept. 1970) p. 56.

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Chalcogenide Alloys

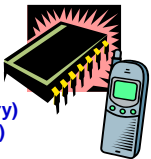
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IVA	VA	VIA	VIIA	
C	N	O	F	
Si	P	S	Cl	
Ge	As	Se	Br	
Sn	Sb	Te	I	
Pb	Bi	Po	At	

↑
Chalcogens

1970 → **Xerography** 

1990 → **DVD-RW
CD-RW** 

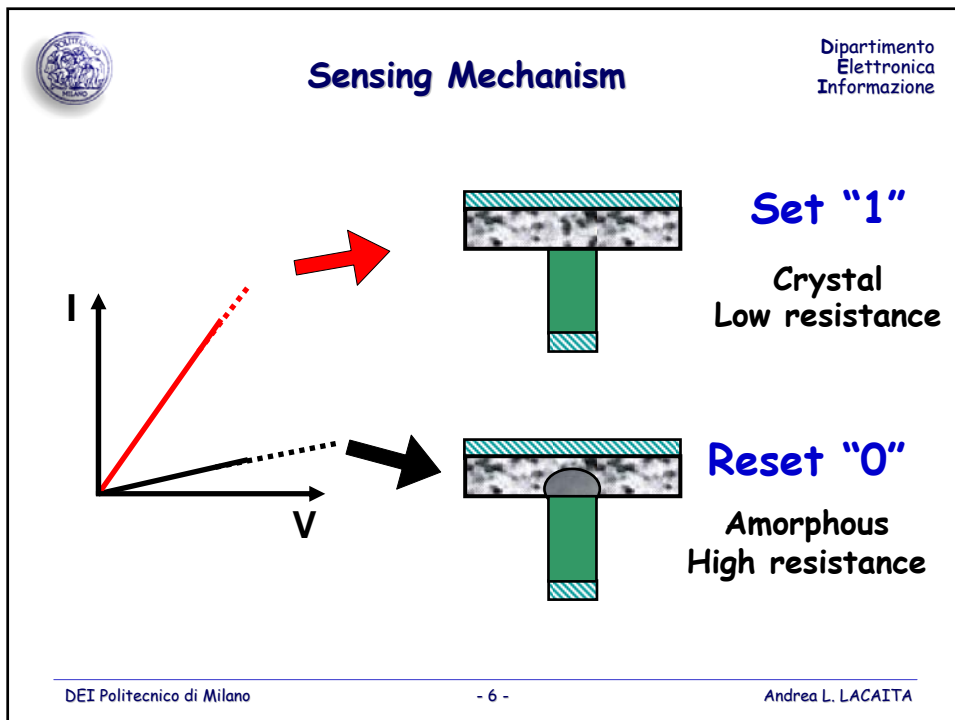
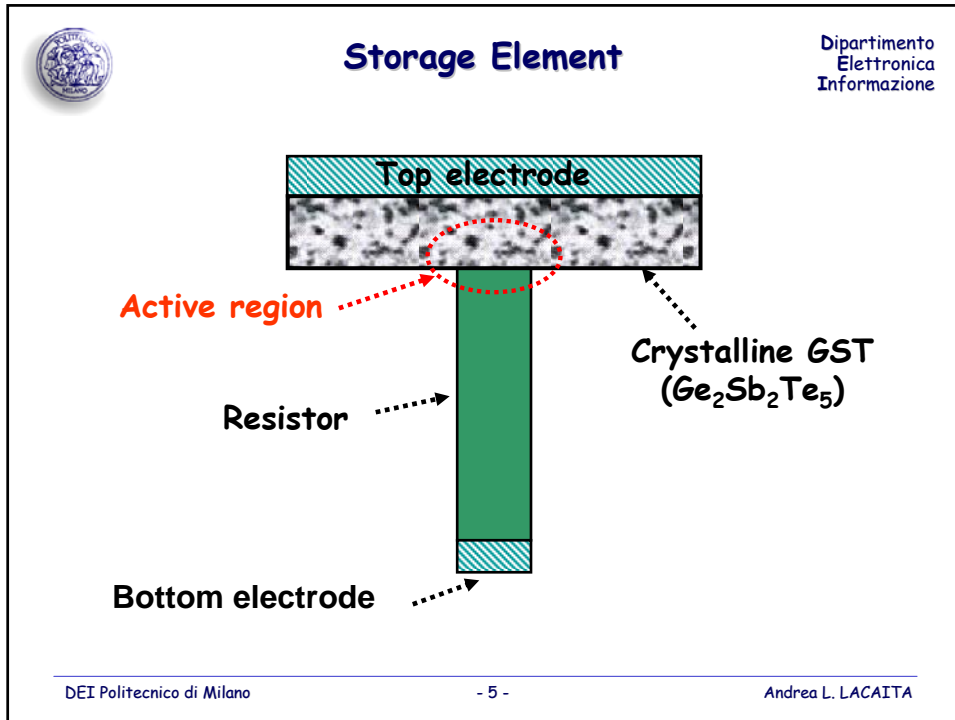
2000 → **Memories** 

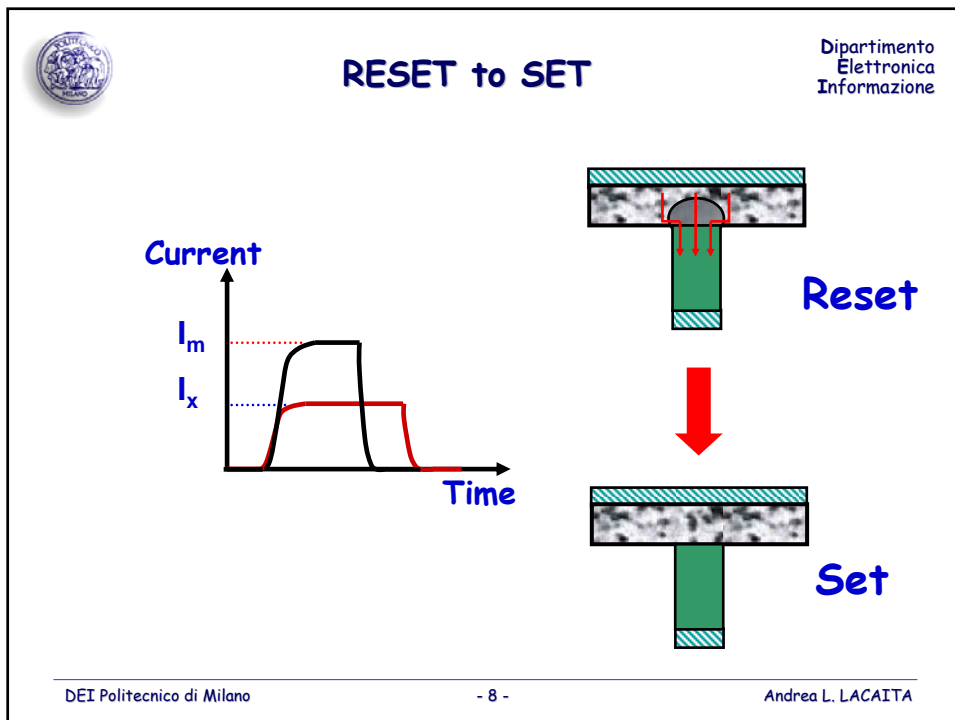
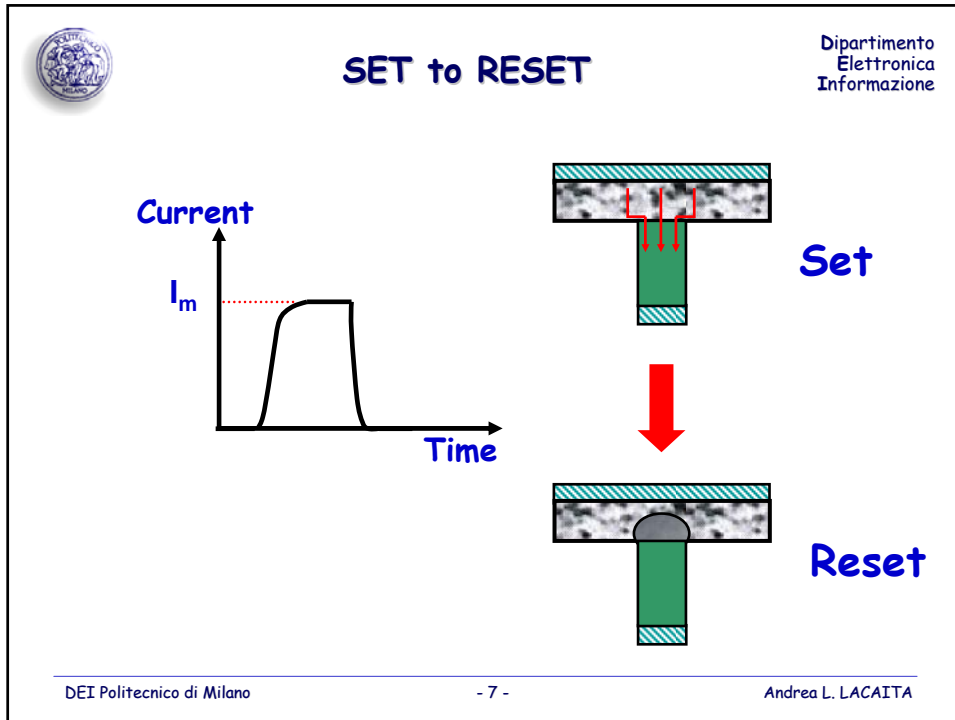
OUM (Ovonic Universal Memory)
 PCM (Phase Change Memory)
 PRAM (Phase-change RAM)

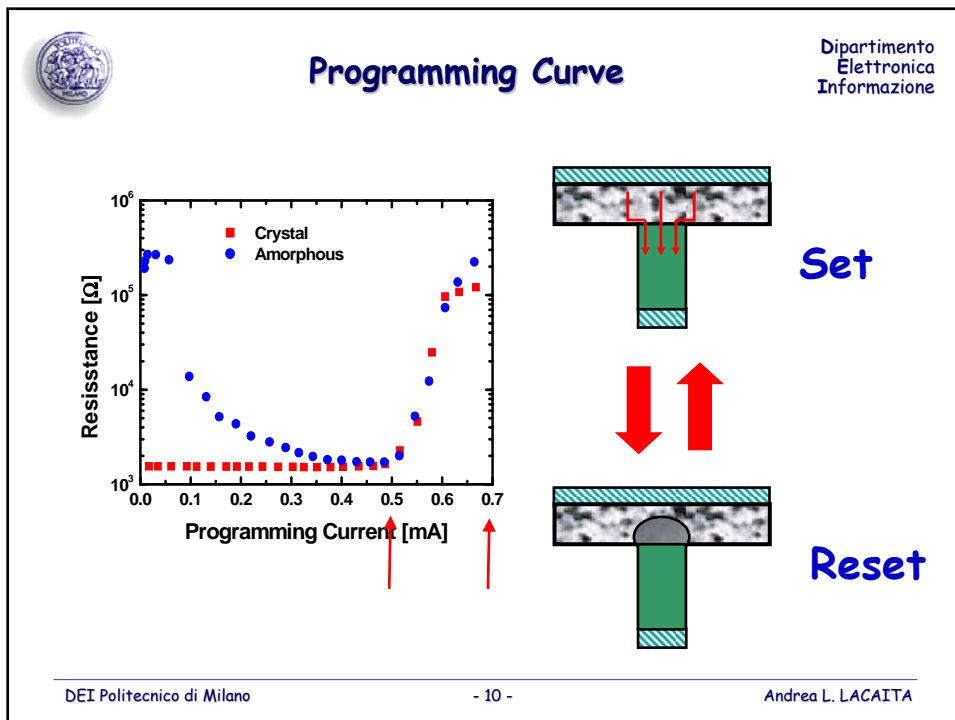
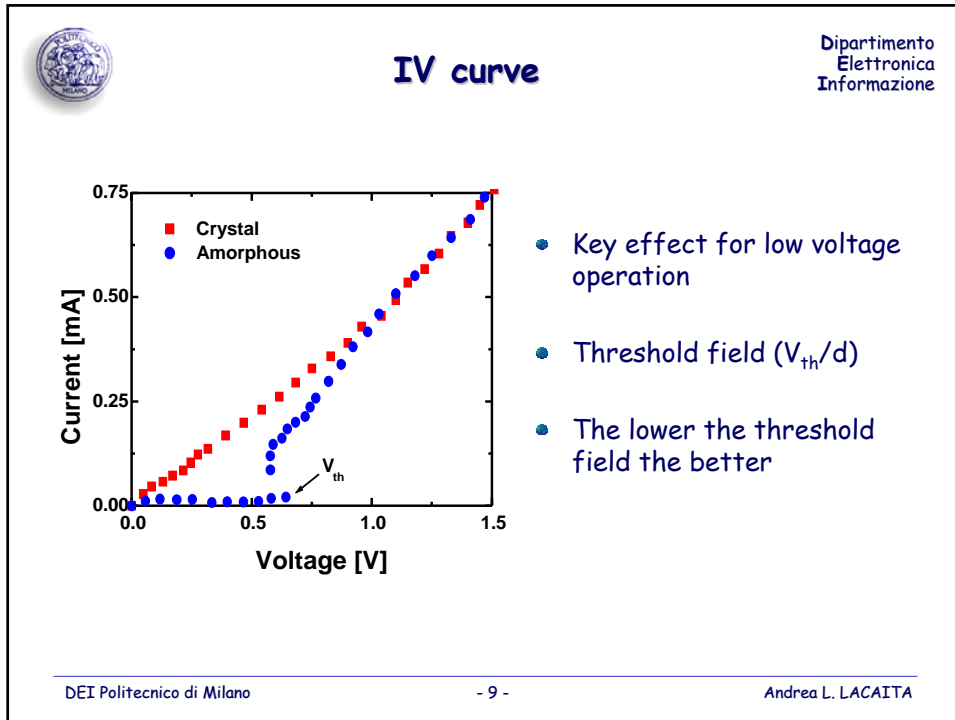
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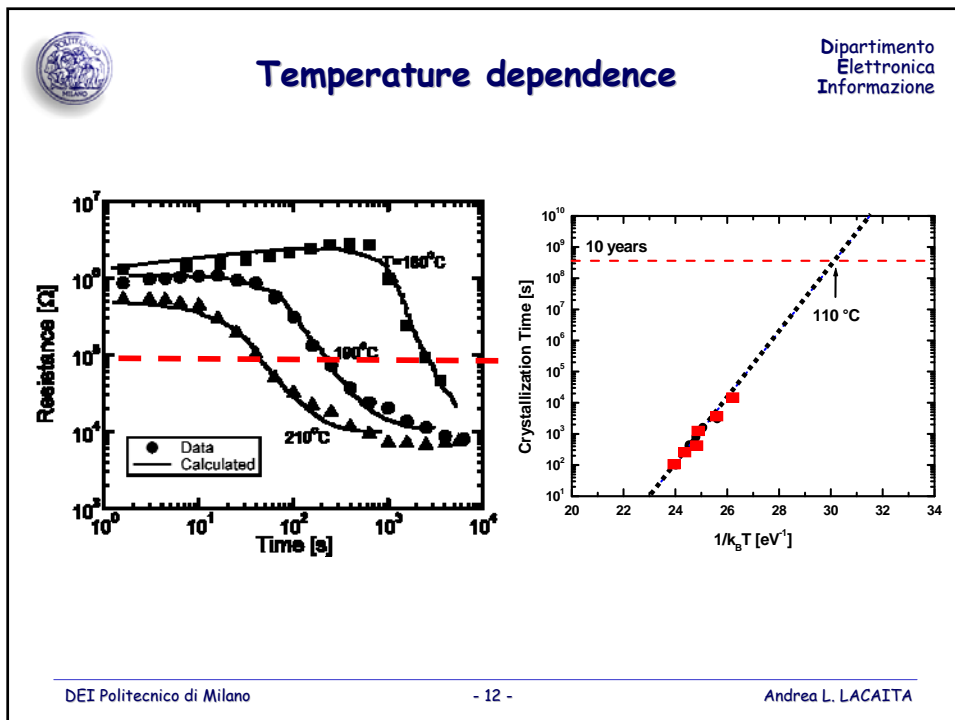
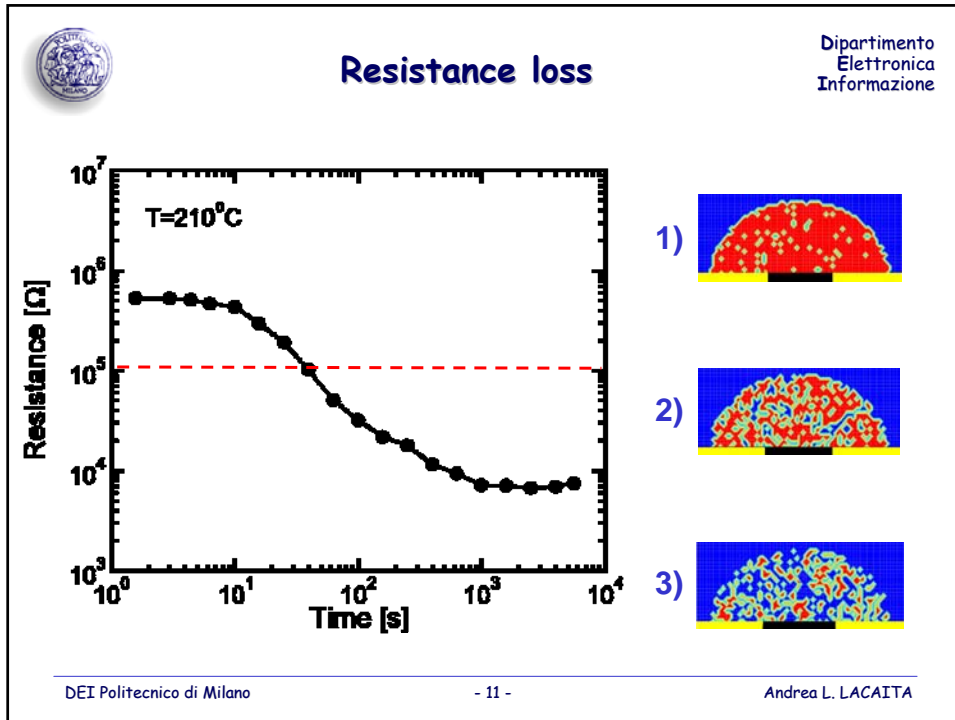
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Material selection rules

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Memory window	resistivity of amorphous phase	high (0.3 MOhm.μm)
Reset Power	resistivity of crystalline phase	high (350 Ohm.μm)
	melting temperature	low (621°C)
Retention	crystallization temperature	high (155°C)
	activation energy	high (2.6-2.9eV)
Bias voltage	threshold field	low (30-40 V/μm)

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Material options

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- Sb_2Te_3 -GeTe GeTe-InTe
 - ▶ higher amorphous stability, better retention
 - ▶ higher maximum operating temperatures
 - ▶ slower

- O/N doped GST
 - ▶ higher resistivity
 - ▶ lower current

- Doped SbTe, GeSb
 - ▶ fast growth materials

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Summary

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- Beyond the capacitive concept
- Fast write (set/reset) and read
- Medium/low voltage write

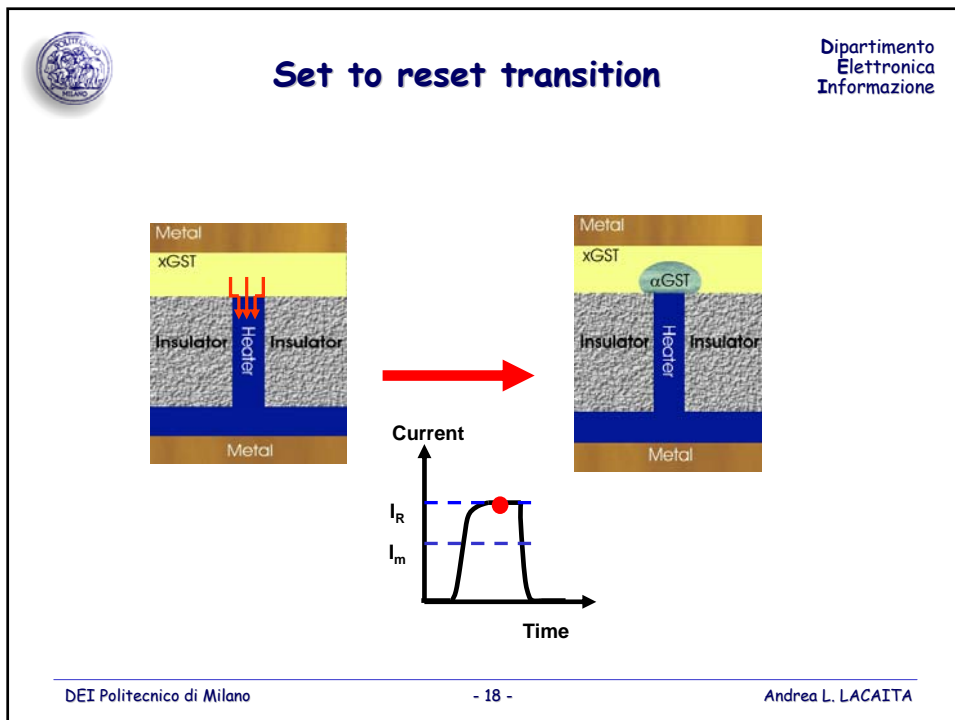
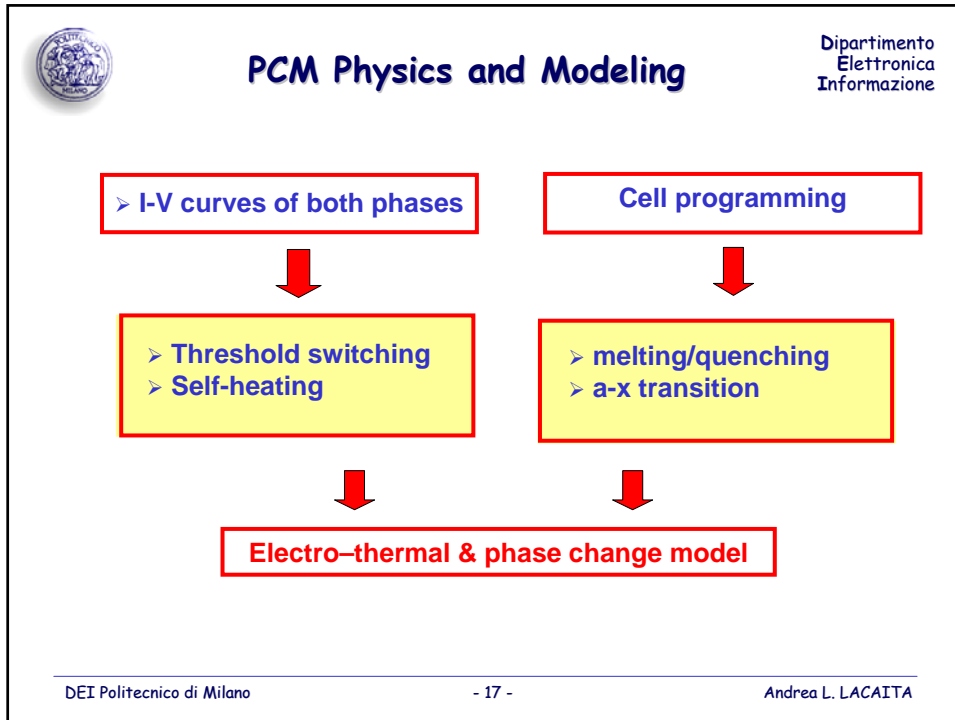
- Supply (threshold field)
- Power consumption (melting temperature)
- Retention (crystallization temperature, activation energy)
- Window (resistivity change)

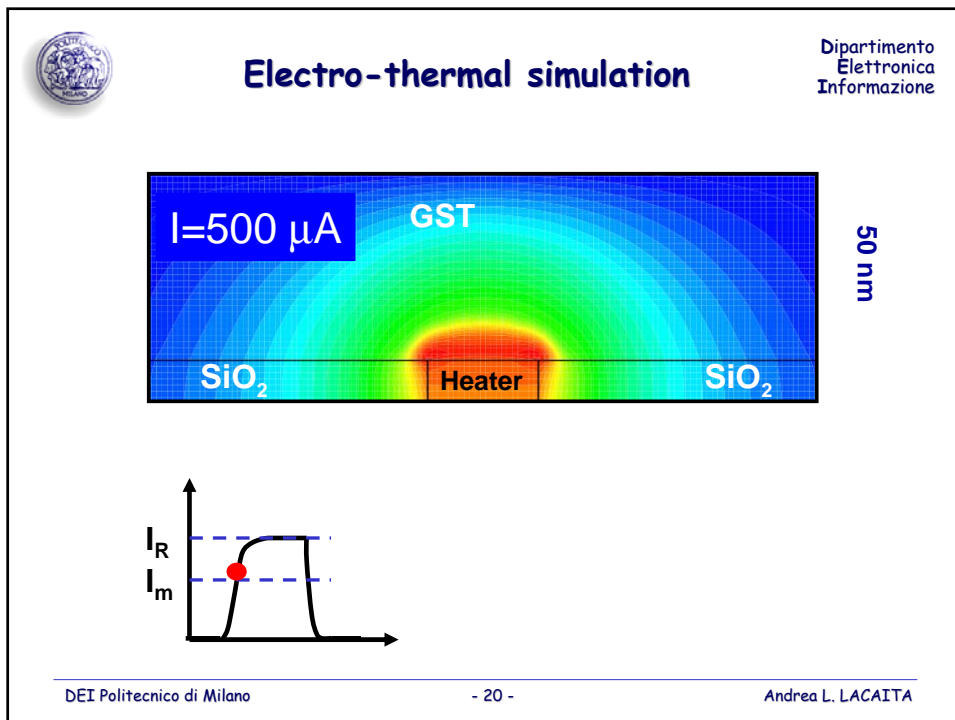
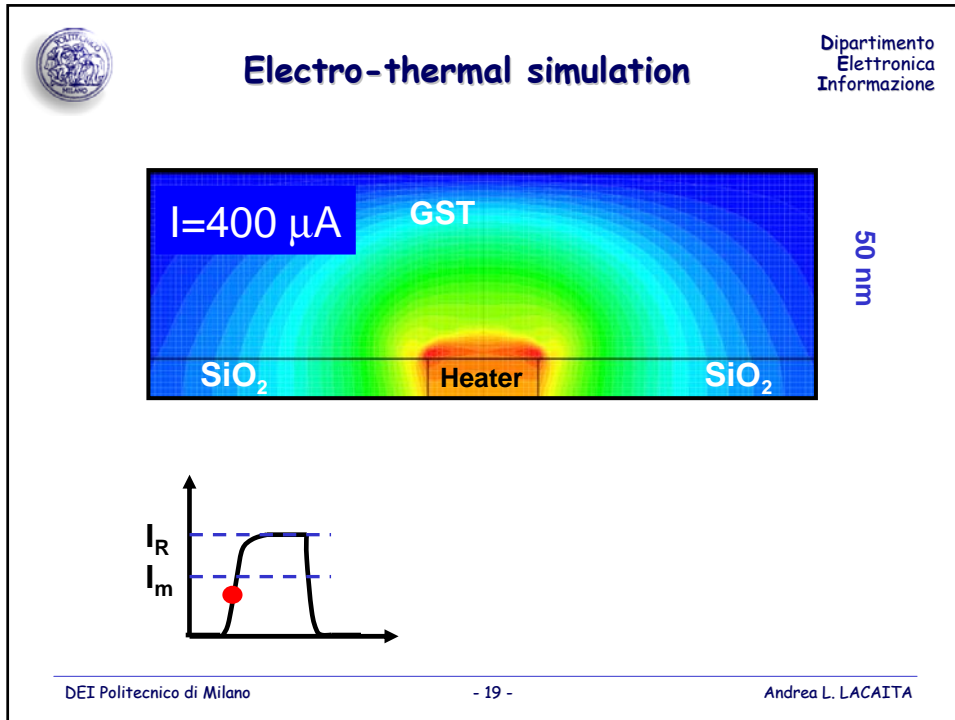


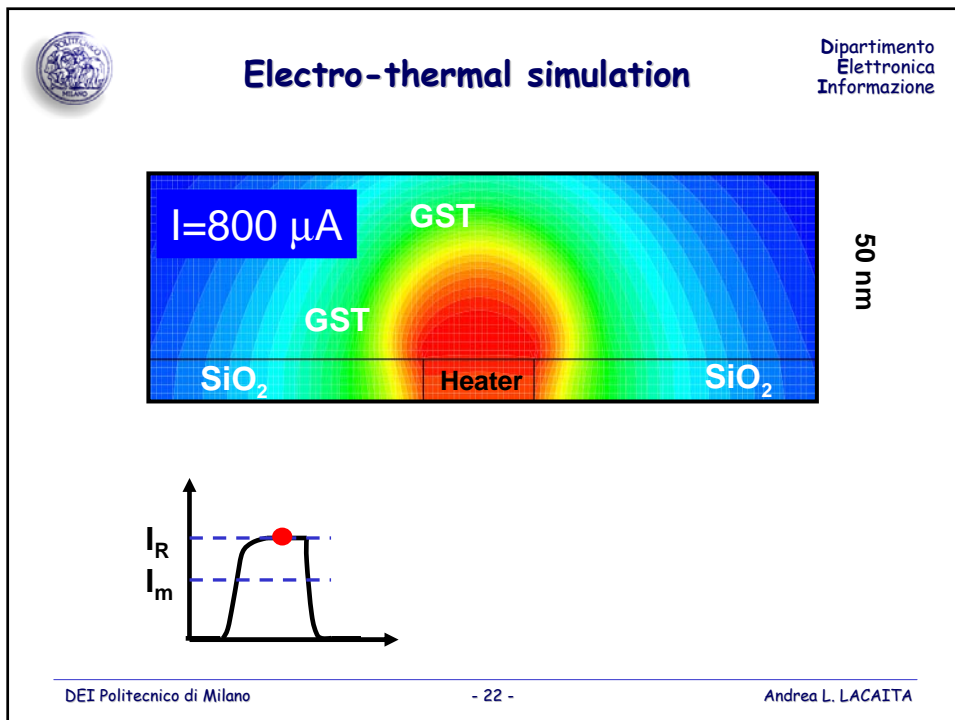
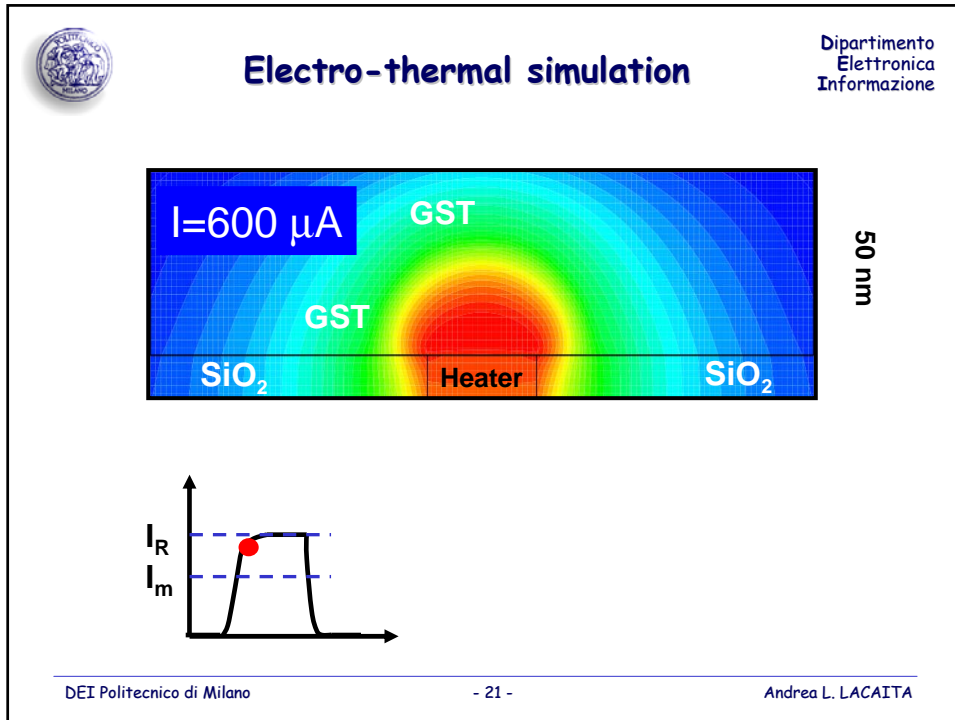
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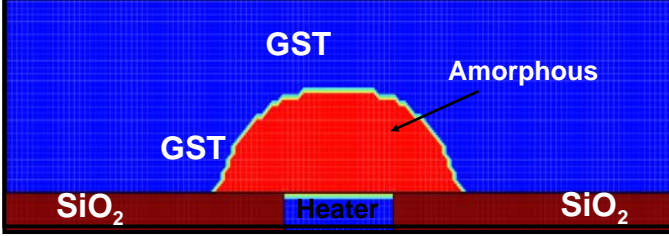


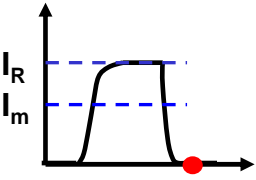




Electro-thermal simulation

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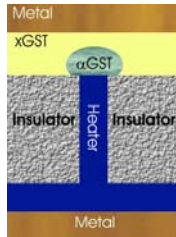
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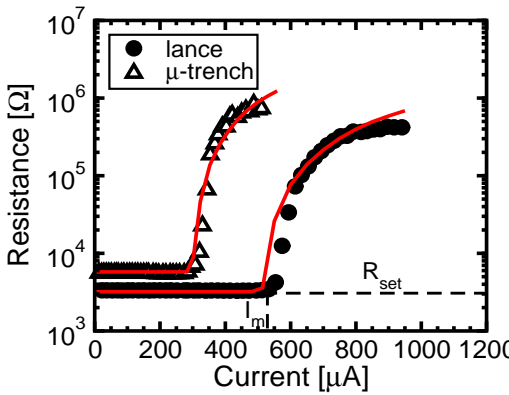
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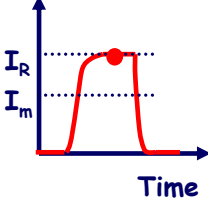


Programming curve

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Material parameters

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$\rho = 17 \text{ m}\Omega\text{cm}$
 $\kappa = 1 \text{ W/Km}$

$\rho = 50 \Omega\text{cm}$
 $\kappa = 0.3 \text{ W/Km}$
+ Wiedemann-Franz
+ Thompson

$\rho = 25 \text{ m}\Omega\text{cm}$
 $\kappa = 12 \text{ W/Km}$

$\kappa = 0.7 \text{ W/Km}$

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Reset to set transition

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Current

Time

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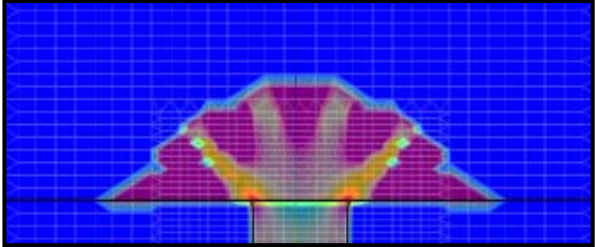
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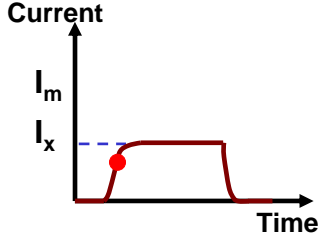


Reset to set transition

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Current



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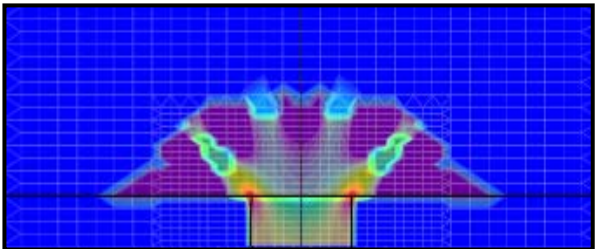
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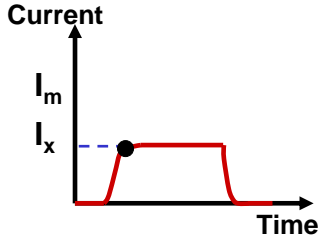


Reset to set transition

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Current



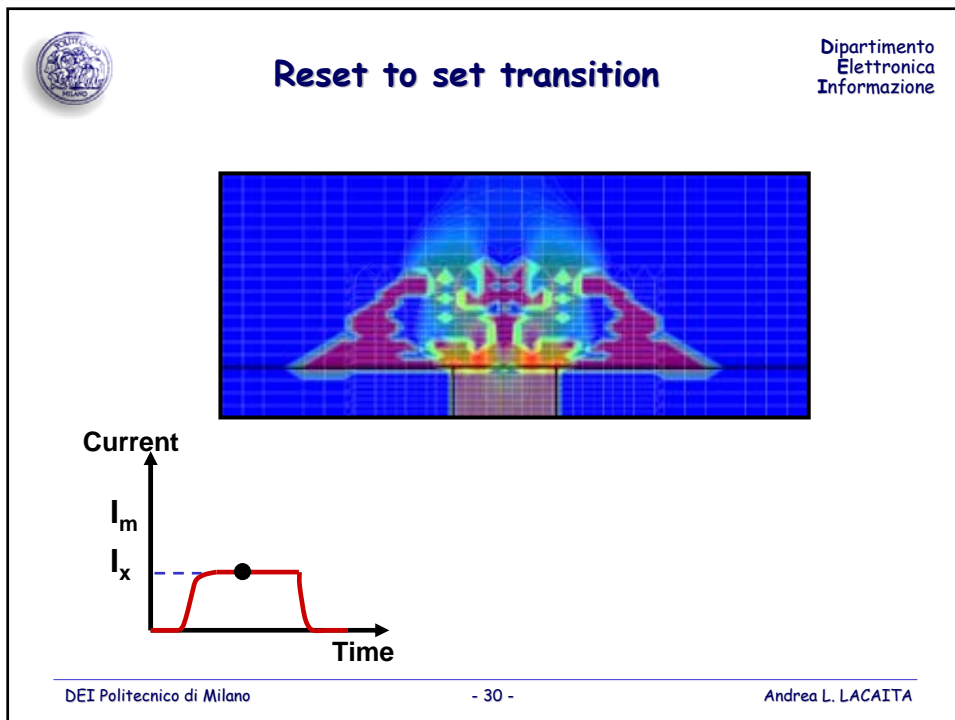
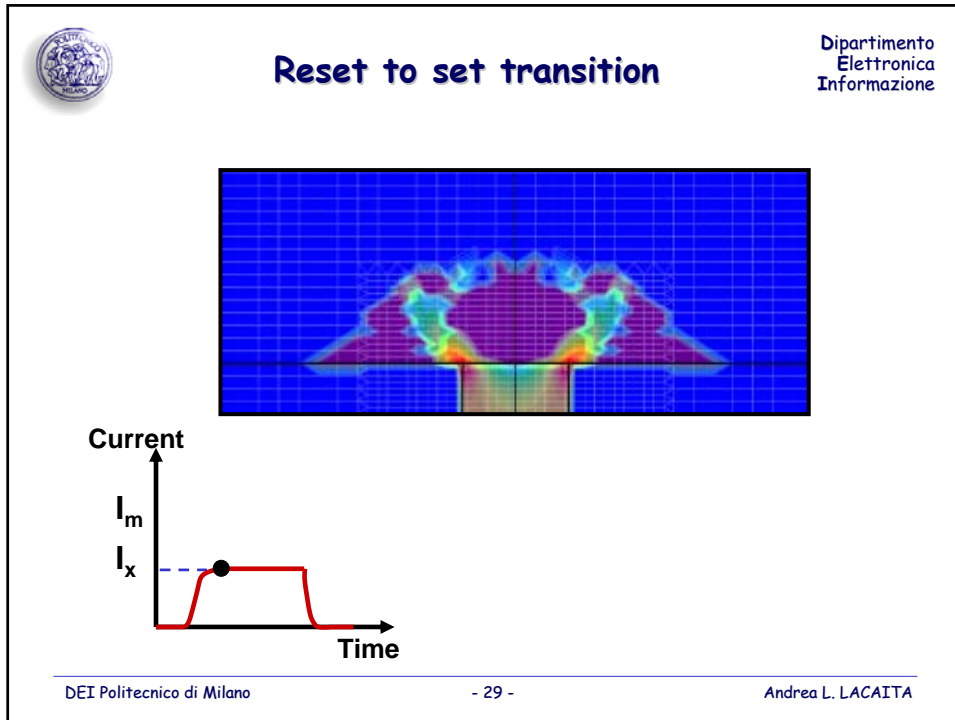
**conduction starts
in narrow filaments**

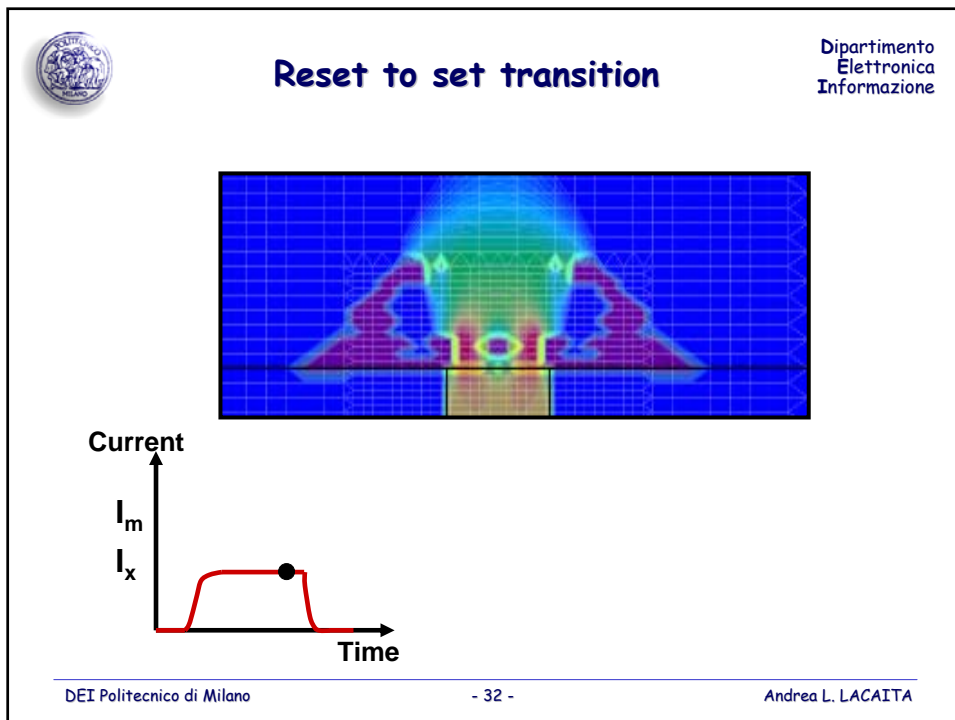
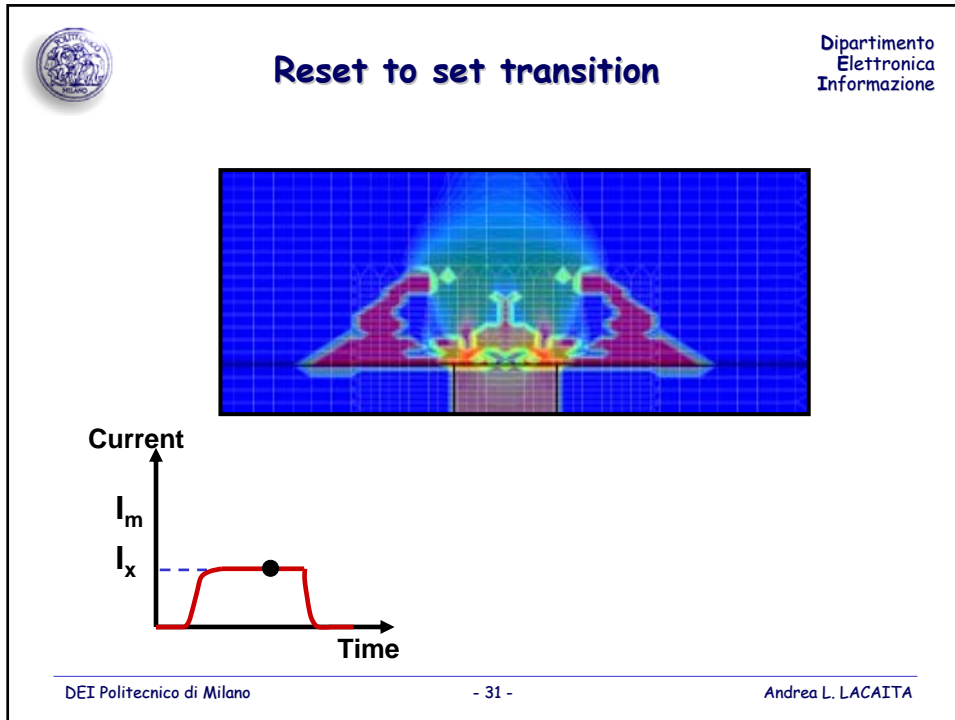
**crystallization takes place
in the same regions**

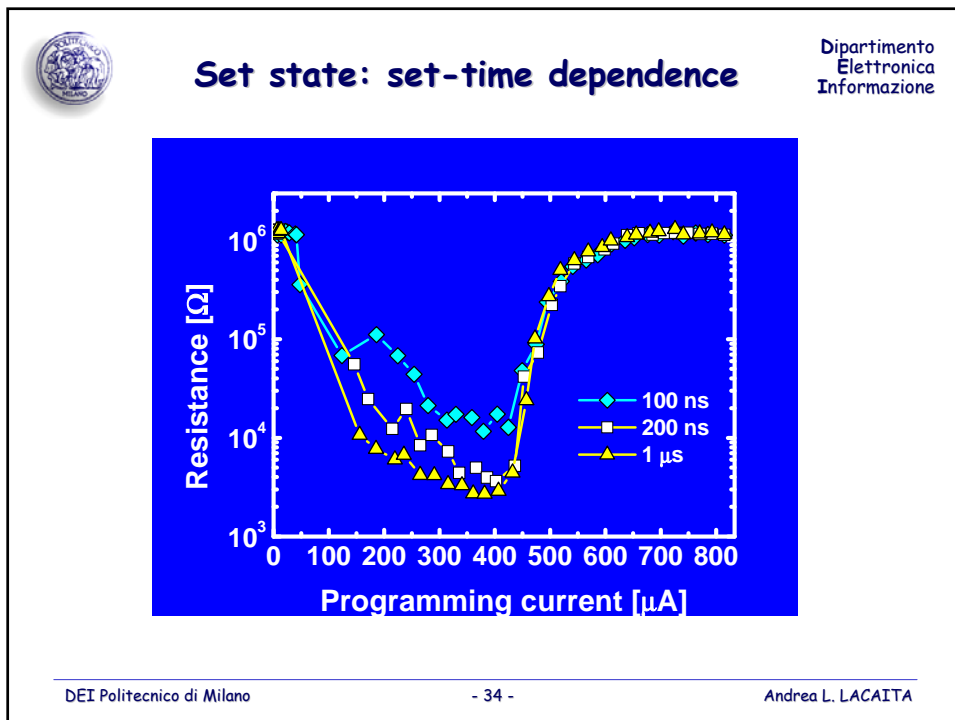
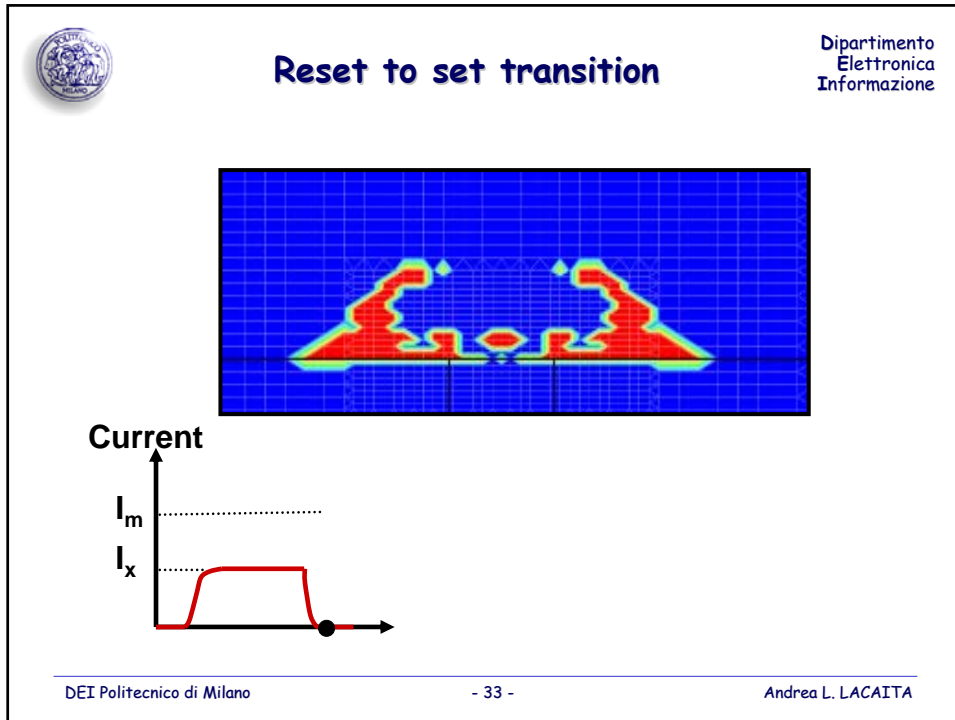
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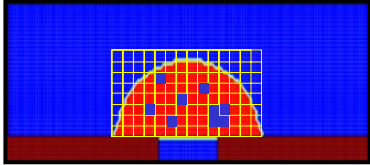






Coupling with crystallization

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Electro-thermal simulation

↓ T_i

Nucleation & Growth

↓


Updated phase distribution

↖ Δt

Transient loop

Nucleation and Growth implemented through a Montecarlo method

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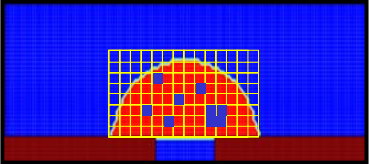
Crystallization

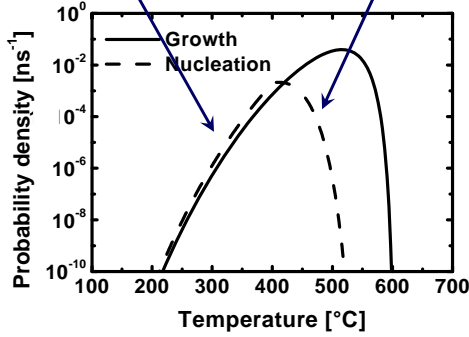
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Thermal enhancement
of atomic mobility

drop of free energy
gain per unit volume

Nucleation - growth





The graph shows Probability density [ns⁻¹] on a logarithmic y-axis (from 10⁻¹⁰ to 10⁰) versus Temperature [°C] on a linear x-axis (from 100 to 700). Two curves are shown: a solid line for 'Growth' and a dashed line for 'Nucleation'. The Growth curve peaks at approximately 550°C, while the Nucleation curve peaks at approximately 450°C. Arrows from the text above point to the respective curves.

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Summary

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- Numerical tools have been developed to support the design and optimization of PCM technology
- Carrier transport and heat flow are self-consistently coupled in the frame of semiconductor device simulator
- Material parameters have been tailored to quantitatively account for experimental results
- These tools are essential to design further scaled cell architectures.



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PCM and Joule heating

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- Endurance
- Cross talk

- Power dissipation / current consumption
 - ▶ 30mA @ 1,8V
 - ▶ Reset current 500µA/cell
 - ▶ Write cycle time 1µs
 - ▶ 16Mb/s = 2MB/s

10mA @ 5V
 20 cells in parallel
 1Mcycles/sec

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Current reduction by scaling

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$$\Delta T_M = P_d \cdot R_{TH}$$

$$P_d = R \cdot I^2$$

1

↓

k

↓

1/k

↓

k

↓


1/k

↓

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PCM scaling strategies

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<i>Parameters</i>		<i>isotropic</i>	<i>anisotropic</i>
GST/Heater contact area	A_{cell}	$1/k^2$	$1/k^2$
Layer thickness		$1/k$	1
Electrical/Thermal Resistances	R	k	k^2
Power dissipation	P_{cell}	$1/k$	$1/k^2$
Current	I	$1/k$	$1/k^2$
Voltage	V_{cell}	1	1
Current density	J	k	1

$$R_{set} \times I_m = const$$

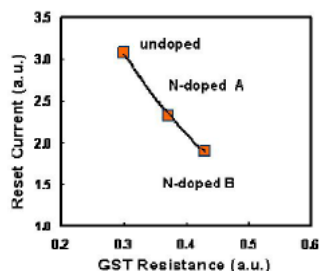
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Current reduction

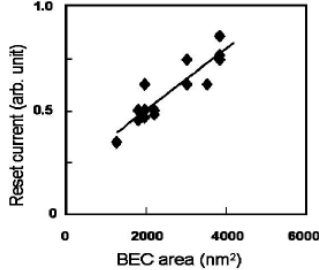
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- by scaling
- by material engineering (active/heater)
- by cell architecture

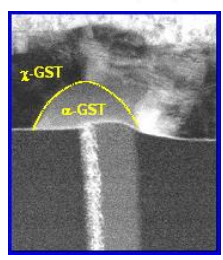


Reset Current (a.u.) vs GST Resistance (a.u.)

Legend: undoped, N-doped A, N-doped B




Reset current (arb. unit) vs BEC area (nm²)



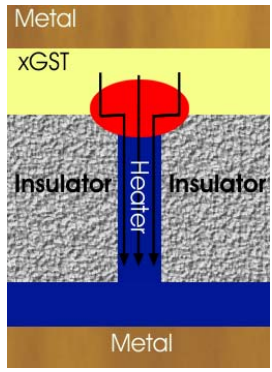
χ -GST
 α -GST

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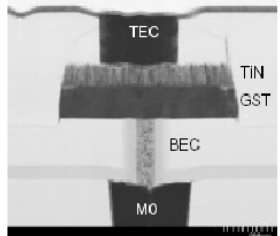


Lance / Ring


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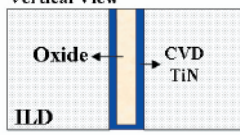
Hori et al. VLSI 2005



Top View




Vertical View



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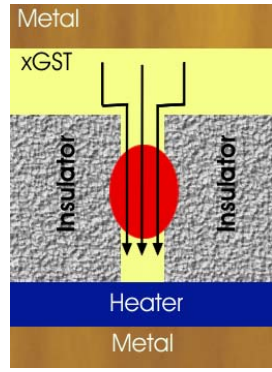
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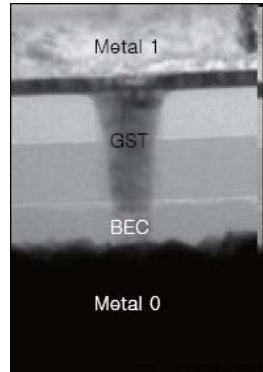
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Pillar / Pore

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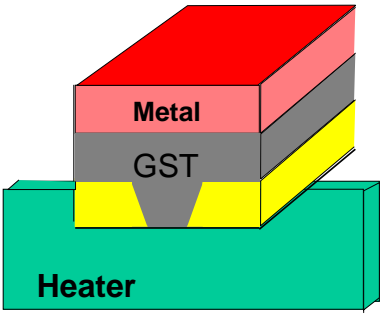
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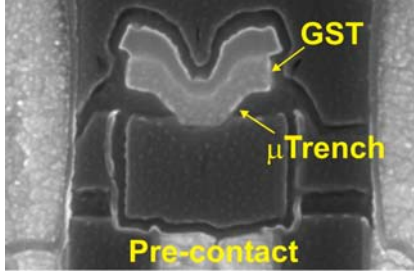


μtrench

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Heater



Pre-contact


F. Pellizzer et al, VLSI'06

- Contact area: heater thickness x sublitho

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Technology benchmarking


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	STM-Intel VLSI 06	Samsung IEDM 06	Hynix J. Sem. Sci. And Tech. 8(2), 128, 2008	Hitachi IEDM06 ISSCC06	IBM- Qimonda- Macronix VLSI 06	IBM- Qimonda- Macronix VLSI 07
F [nm]	90	90	90	130	180	180
Cell type	μtrench/ lance, bipolar,	Ring, GST N-doped, diode, 5,8F ²	-	Lance, GST -Ta ₂ O ₅ layer, MOSFET	Pillar, GST N-doped MOSFET	Pore, GST N-doped MOSFET
Ireset [mA]	0.4/0.7	0.6	1.0	0.1	0.9	0.4
Array size [# bit]	128M	512M	512M	4M	Mini array	256k
Set time [ns]				1200	300 (MLC)	80
Endurance [#]	>10 ⁸	10 ⁵		10 ⁶	10 ⁶	10 ⁵

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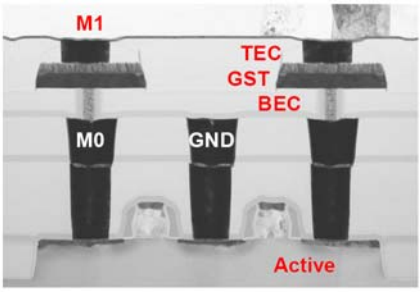
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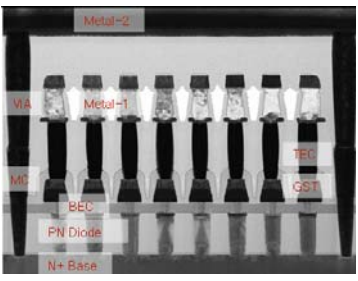


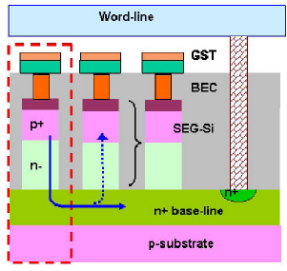
From MOSFET's to diodes

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Samsung, VLSI'04






Samsung, IEDM'06

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Summary


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- Among the various candidates for future NVMs, PCM technology has shown the most convincing prospects for commercial products
- High density arrays as well as embedded solutions have been successfully demonstrated
- Short-term: valuable solution for embedded applications, code storage, high performance memory systems
- Long-term: solution for data storage applications

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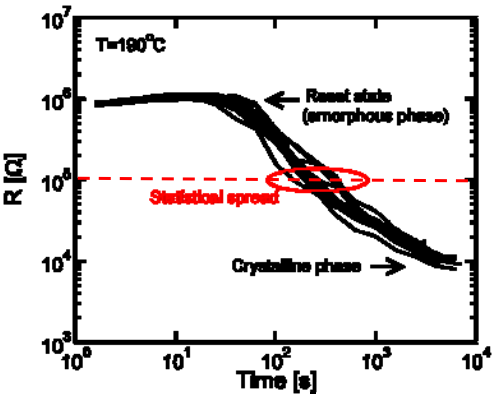
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Data-loss statistics

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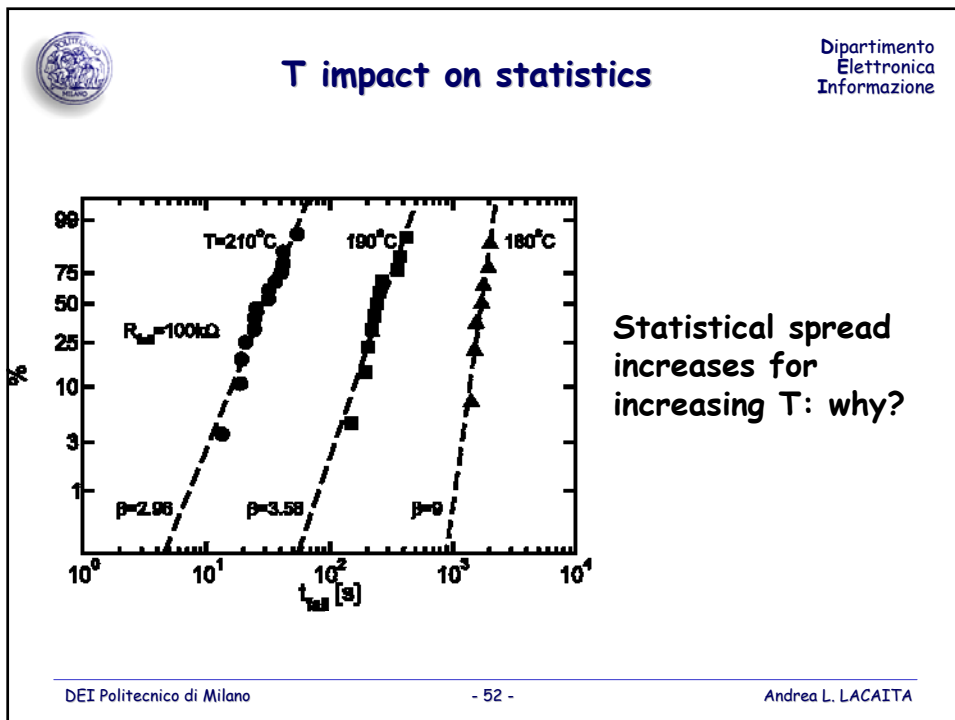
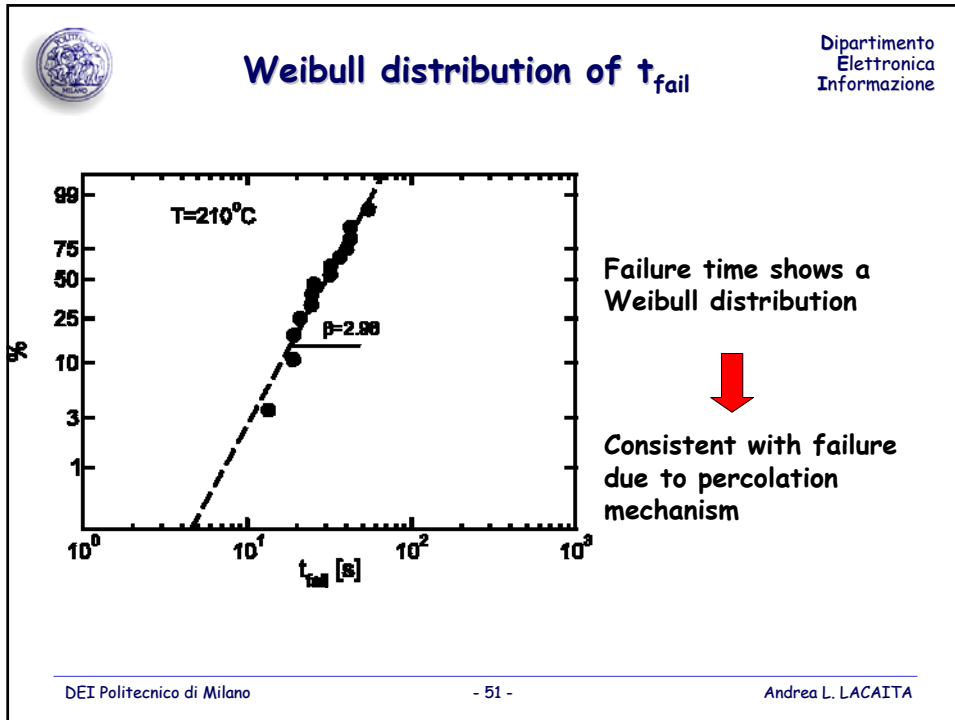


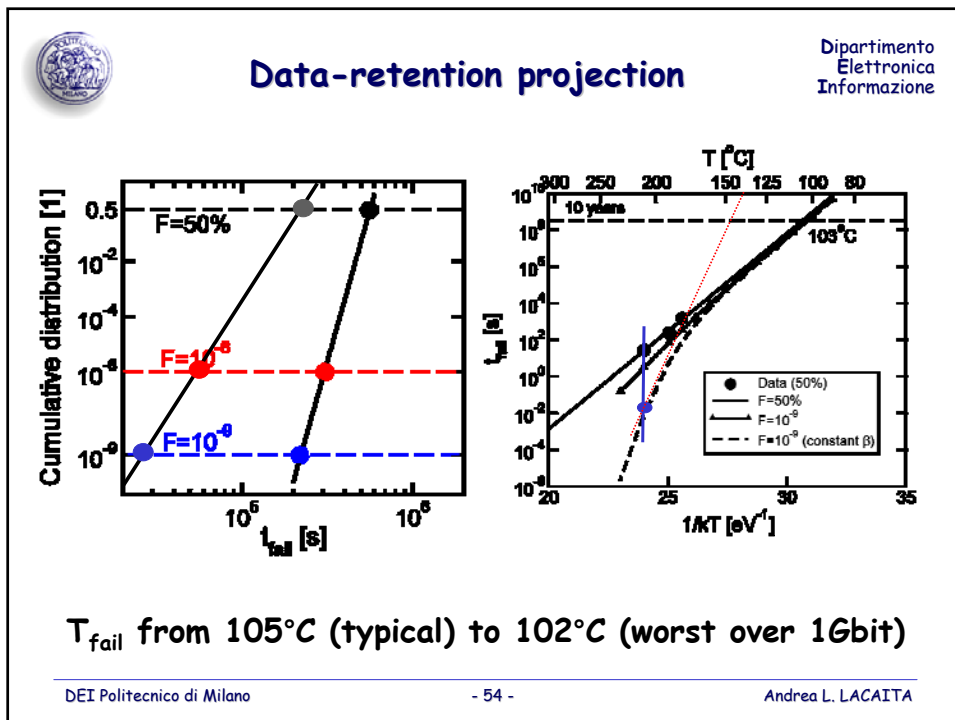
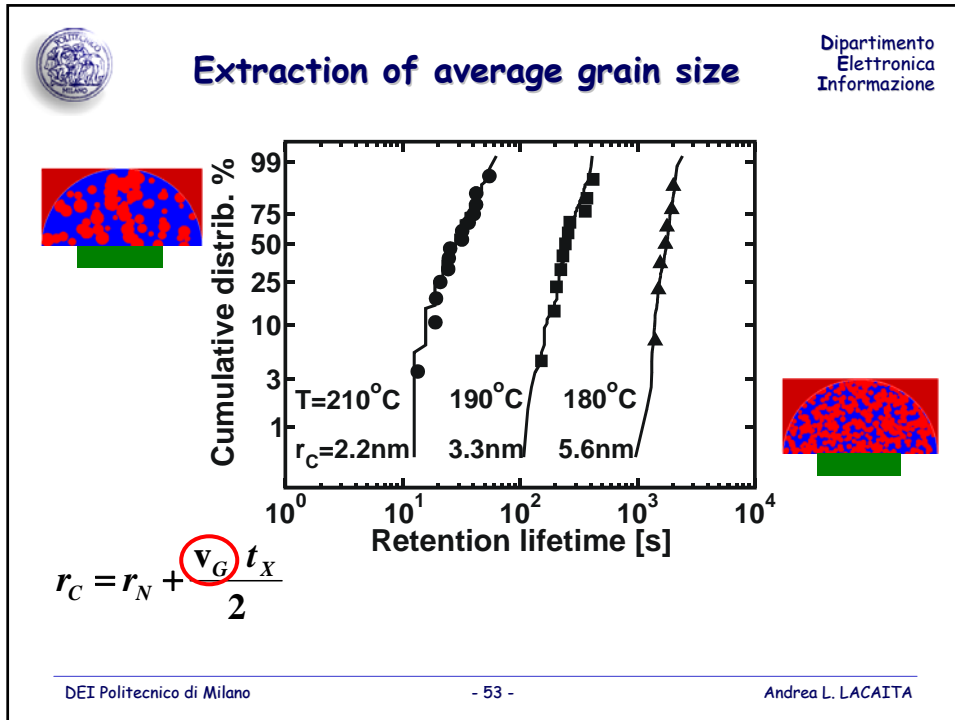
Repetitive measurements on the same cell show statistical spread

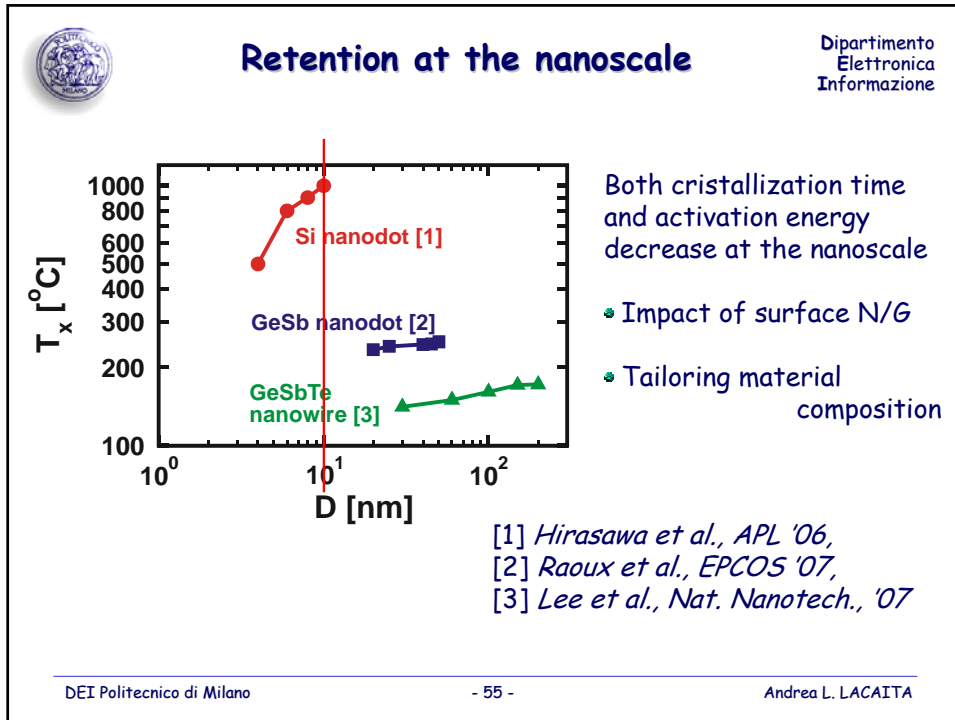
↓

data loss is erratic

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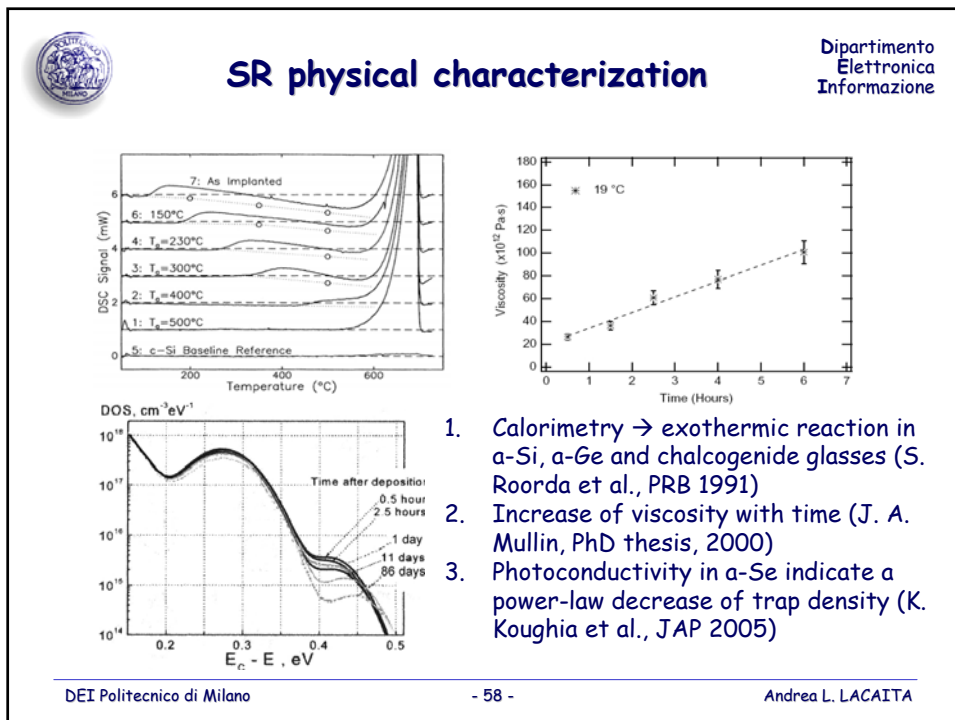
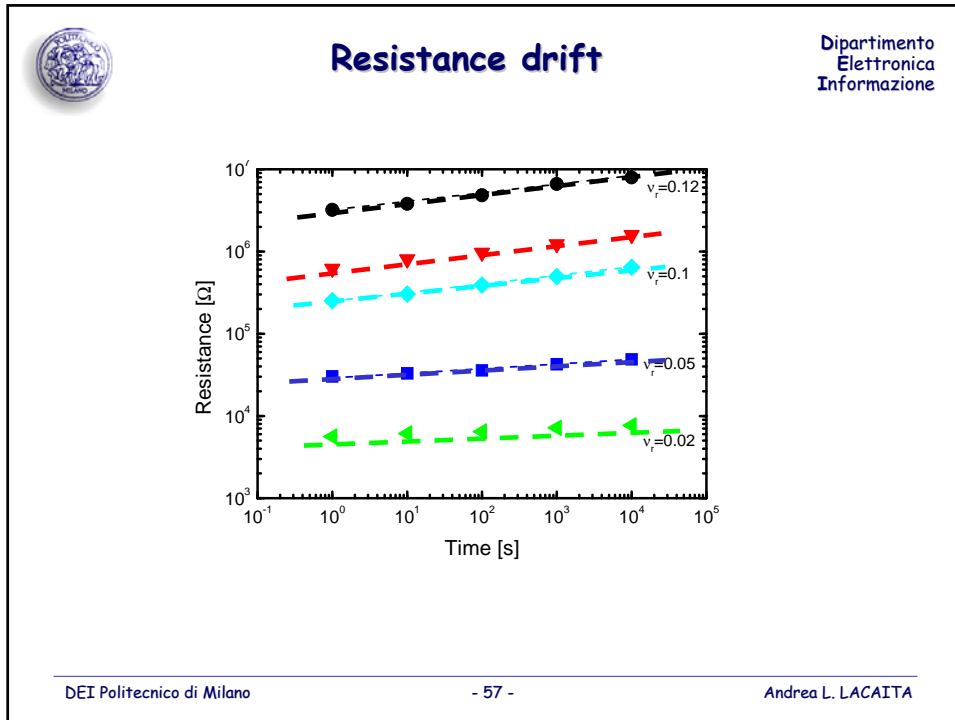



Reliability issues

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Reliability issue	Impact on Cell
Crystallization	Resistance decrease
Structural relaxation	Resistance increase
Cycling endurance	Stuck set/reset
Program disturb	Resistance decrease/increase
Read disturb	Switching and resistance decrease

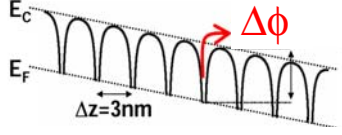
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Poole-Frenkel conduction

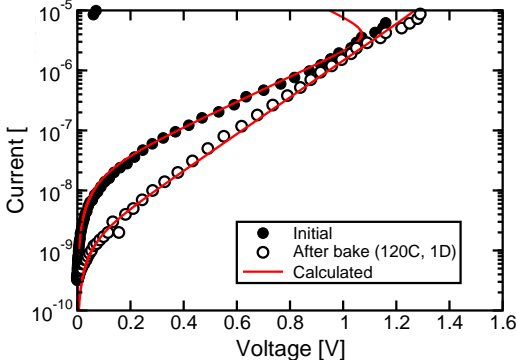
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Less defects

Lower current

Higher resistance




Ielmini et al., IEDM'07

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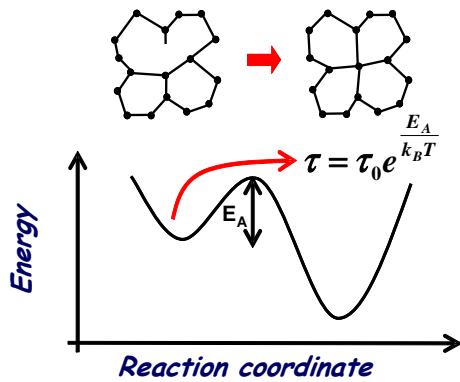
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Kinetic model for SR

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- SR is due to atomic rearrangements in the disordered structure
- kinetic reproduced by metastable defect relaxation with broad distribution of activation energies
- Material engineering
- Programming/reading schemes to minimize the effect

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Summary

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- Perspectives of PCM at the nanoscale calls for optimization/engineering of material properties
- Drift and defects dynamics, intrinsically linked to the amorphous phase has to be faced and dominated to make reliable MLC.
- Great fun in the next future!



Acknowledgments

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